ULTRA-THIN POLYMER DIELECTRIC MATERIALS AND ULTRA-SMALL VIA AND TRENCH PROCESSES FOR 20MICRON BUMP PITCH RE-DISTRIBUTION LAYER (RDL) STRUCTURES FOR HIGH DENSITY PACKAGES

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by

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LIST OF SYMBOLS AND ABBREVIATIONS

I/O	Input and output
BEOL	Back end of line
RDL	Re-distribution layer
TSV	Through silicon via
PWB	Printed wiring board
CTE	Coefficient of thermal expansion
Tg	Glass transition temperature
eWLP	Embedded wafer level packaging
FO-WLP	Fan-out wafer level packaging
HD-FO	High density fan-out wafer level packaging
CVD	Chemical vapor deposition
PVD	Physical vapor deposition
HDP	High density plasma
RIE	Reactive ion etching
CMP	Chemical mechanical planarization
SAP	Semi-additive processes
CoO	Cost of ownership

TSR	total strain range
HAST	Highly accelerated stress tests
FEM	Finite element modeling
TTV	Total thickness variation
NP	Norbornene type polymer

SUMMARY

Higher interconnect density between multiple chips is required because of the need for higher bandwidth data transmission for many electronic systems, such as smart mobile devices, cloud and edge computing, and in machine learning in autonomous driving and robotics. Although side-by-side integration with 2.5D silicon interposers with back end of line (BEOL) wafer processes have enabled the high input-output (I/O) density interconnections, they have challenges in electrical performance and cost. Meanwhile, organic package substrates have higher electrical performance and low cost capability, however, they have been unable to bridge the I/O pitch gap from 80 µm to 20 µm, because of the dimensional instability and warpage.

The objectives of this research are to explore and demonstrate ultra-thin dry film polymer materials, processes and lithographic structures to form copper-polymer re-distribution layers (RDL) with silicon wafer-like interconnection densities, but at lower resistance and at lower cost. This research is focused on addressing the limitations of current approaches by; (a) design and demonstration of a novel ultra-thin RDL dielectric material that satisfies the properties for RDL with scalability of conductor wiring to 2 µm by SAP, and (b) investigation of an innovative embedded trench process with fly-cutting planarization tool to achieve 5 µm diameter micro-vias, and 2 µm wiring traces with high positional accuracy at ±1-2 µm. Detail design of the dielectric thickness was based on the 50 ohm impedance matching calculation and thermo-mechanical finite element modeling approach. Additionally, new dielectric materials with excellent properties were introduced and in-depth analysis of their electrical, thermo-mechanical and adhesion

properties were performed. To develop the RDL wiring process, a new embedded trench formation process was developed using parallel mask projection processes and an innovative planarization process to address the challenges of RDL scaling with current processes.

CHAPTER 1. INTRODUCTION

1.1 Motivation and Background

The objectives of this research are to explore and demonstrate ultra-thin dry film polymer materials, processes and lithographic structures to form copper-polymer re-distribution layers (RDL) with silicon wafer-like interconnection densities, but at lower resistance and at lower cost. Such a technology will address the interconnect density gap between the current semiconductor back end of line (BEOL) wafer processes that use vacuum deposited thin films with high capacitance and resistance, and build-up organic package substrate panel processes that use much thicker polymer dielectric films with large via and line dimensions above 10 μm. The need for higher interconnect density between multiple chips is driven primarily by the high bandwidth data transmission required in a number of electronic systems, including smart mobile devices, cloud and edge computing, and in machine learning in autonomous driving and robotics. Although direct chip stacking using 3D through silicon via (TSV) interconnections provides the highest bandwidth between logic and memory ICs, thermal and yield challenges have forced the adoption of side-by-side integration using 2.5D interposers as the front-up approach with high input-output (I/O) density interconnections between processor and stacked memory ICs on the same substrate. The first 2.5D interposers were based on silicon wafers with BEOL RDL, reducing the I/O pitch from 80-150 μm used in organic flip-chip package substrates to 40 μm for die to die wide I/O channels. The I/O pitch for 2.5D interposers is expected to shrink to 20 μm pitch and below in the next five years. To connect multiple ICs at such fine pitches with thousands of interconnections, the RDL

wiring needs to be scaled from current package substrate design rules of 10-15 µm to 2 µm for copper line widths and spaces, and from 30-50 µm diameter to less than 10 µm diameter for layer to layer micro-vias. An example of the line widths and spaces, as well as the micro-via pad diameters required to route signals in and out of ICs at 20µm bump pitch is shown in Figure 1.1.

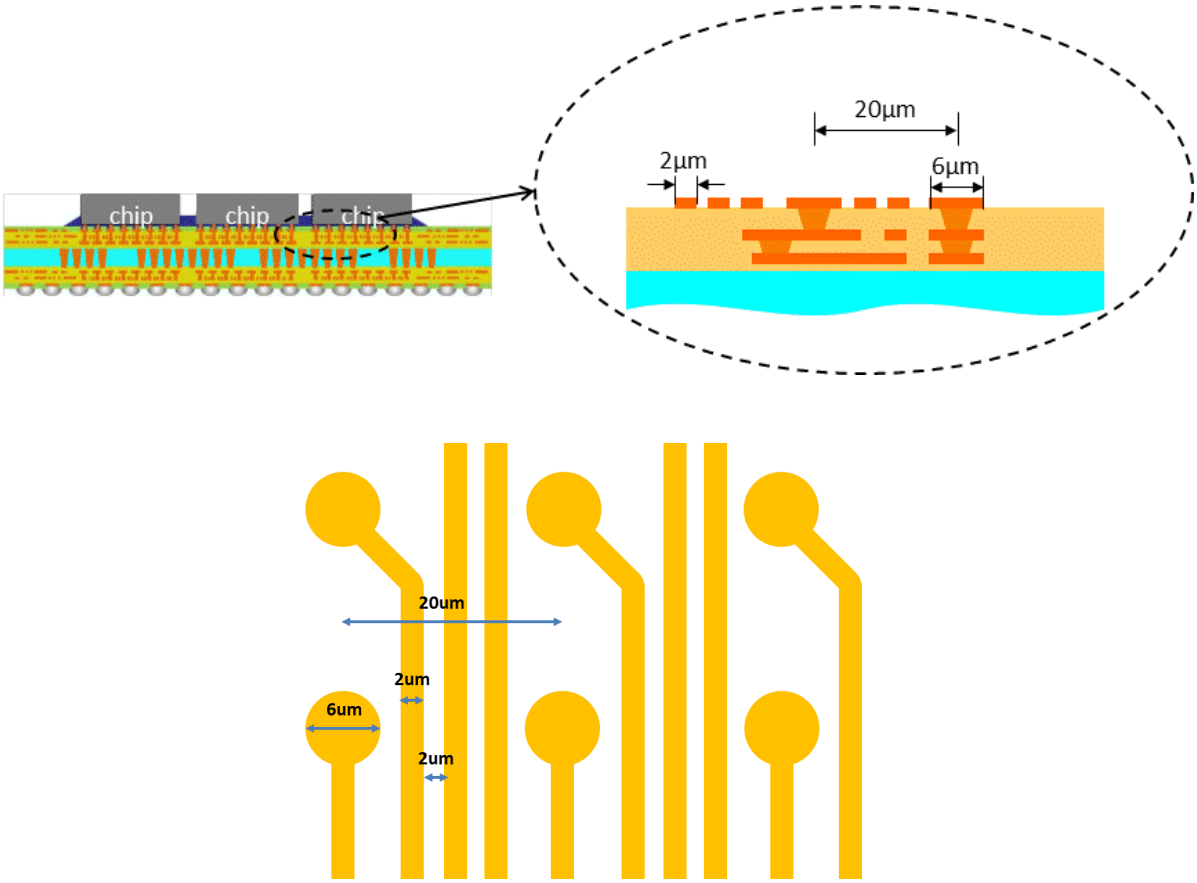

Figure 1.1 RDL routing design with 2 µm conductor widths and spaces and 6 µm via capture pads for interconnecting future 2.5D multi-die interposers

Current organic package substrates use fiberglass reinforced epoxy composite laminate materials as the core, thick epoxy films as inter-layer build-up dielectrics and

copper wiring structures using printed wiring board (PWB) fabrication processes. The polymer-glass composite laminate cores used in these build-up package substrates have migrated to lower coefficients of thermal expansion (CTE) to improve the CTE match to silicon ICs with a CTE of 3 ppm/°C. Another trend in organic laminate cores is the move to higher glass transition temperatures (Tg) to improve the thermal and dimensional stability during the process temperature cycles, and to achieve smaller pitch wiring. Package substrates are fabricated in 510 mm square size panels using epoxy-based dry film interlayer dielectrics with a typical thickness of 20-40 μm per layer, with 30-50 μm micro-vias formed by sequential CO_2 laser ablation, and 10 μm conductor trace widths. Organic package substrates have been unable to bridge the I/O pitch gap from 80 μm to 20 μm, limited by several fundamental challenges, including dimensional instability during thermal process excursions, and warpage due to their low elastic modulus, in spite of the material advances in recent years. Hence, silicon interposers using BEOL wafer processes were developed to interconnect logic and memory chips at high bandwidths, currently reaching 256-512 GB/s. The copper wiring structures on silicon interposers made by BEOL processes on 300 mm round wafers, form sub-micron RDL structures such as conductor traces and layer-to-layer micro-via interconnections [1]. Although silicon interposers meet the fine pitch interconnection requirements, they have two main challenges, namely, electrical performance and cost. The signal loss and line resistance in the thin conductive metallization (up to 1 μm thick) is large, and the sub-micron dielectric films also cause high line capacitance, limiting high speed performance. The cost of BEOL materials and processes is high, limiting the application of silicon interposers to high end products.

Recently, embedded wafer level packaging (eWLP) or fan-out wafer level packaging (FO-WLP) technologies have been developed with 2 μm line width and space wiring [2, 3]. High density fan-out wafer level packages (HD-FO) use copper-polymer thin film wiring with liquid spin-on dielectrics with wafer processes. Although this approach addresses some of the limitations of silicon BEOL and organic packages, they face challenges in forming planar multilayer structures due to the conformal nature of liquid polymer dielectrics. Since these technologies utilize high volume manufacturing tools for semiconductor wafers, they are also limited in package sizes to the 25 mm size of single rectiles. However, future interposers need increasing number of chips on one interposer, resulting in interposer or package sizes as large as 50-60 mm. Since BEOL as well as eWLP and FO-WLP processes from silicon wafer fabs are not scalable to large panels, there is a critical need for panel scalable and high density RDL processes to enable larger body size and lower cost interposers.

1.2 Current RDL Materials and Processes

This section describes the RDL materials and processes for the conductor wirings and micro-vias for BEOL, package substrates, and eWLP/ FO-WLP.

1.2.1 BEOL Materials and Processes

1.2.1.1 Dielectric Materials for BEOL

BEOL RDL processes use chemical vapor deposition (CVD) to deposit ultra-thin films of low k porous dielectric materials. Originally, thermally oxidized SiO_2, whose

dielectric constant Dk is about 4.2, has been used for RDL dielectric layers. As the RDL dimensions have decreased, reduction of capacitance between the RDL wirings became a critical issue, and fluoride doped SiO_2 with lower Dk (3.4-3.7), was introduced from 400 nm technology node. From 90 nm technology node, SiOC has been used as a RDL dielectric material due to the smaller Dk (2.6-2.9). From 45 nm technology node and beyond, porous low k dielectric materials with Dk of 1.9-2.5 have been applied. Such porous dielectric materials have much poorer mechanical stability and are susceptible to the damage induced by later processing such as resist poisoning, plasma damaging, and chemical mechanical polishing [4]. Variety of additional processing technologies to address these challenges such as EB beam curing to improve mechanical strength have been developed [5]. Additional to the dielectric materials, shrinking conductor widths have required higher step coverage during dielectric layer deposition. Hence, high density plasma (HDP) processes were introduced to form dielectric layers with higher step coverage [6]. For the same reasons, seed metal formation by physical vapor deposition (PVD / sputtering) was replaced by CVD.

1.2.1.2 Conductor Wiring and Micro-via Processes in BEOL

Aluminum was the original conductor material for BEOL due to its relatively low electrical resistance and ease of patterning by reactive ion etching (RIE), as illustrated in Figure 1.2.

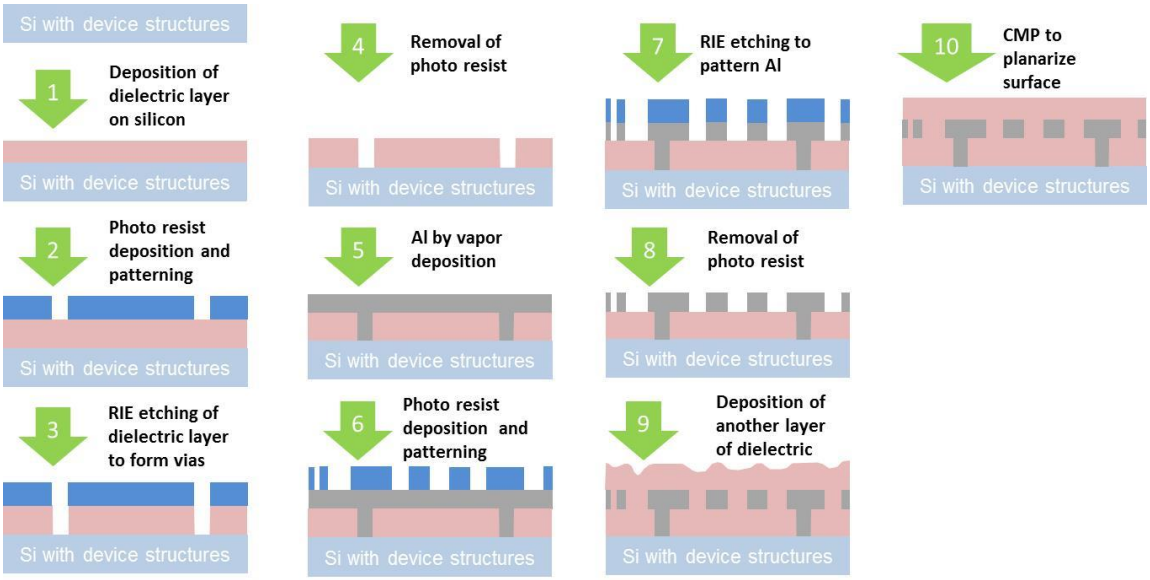

Figure 1.2 Aluminum RIE process for BEOL

Transition of aluminum to copper occurred late 1990s, driven by the need for lower conductor loss and higher resistance to electro-migration [7]. The biggest challenge in this transition was fine structure patterning of copper, because copper cannot be patterned with RIE processes, necessitating the development of new patterning processes. As a consequence, damascene/ dual-damascene processes (Figure 1.3) were established, where the dielectric layer is patterned by RIE to form trenches and vias first, then copper is filled inside by electrodeposition, followed by chemical mechanical planarization (CMP) to remove the copper overburden. Ultra-small line and via structures with 100 nm size can be achieved using the dual-damascene processes.

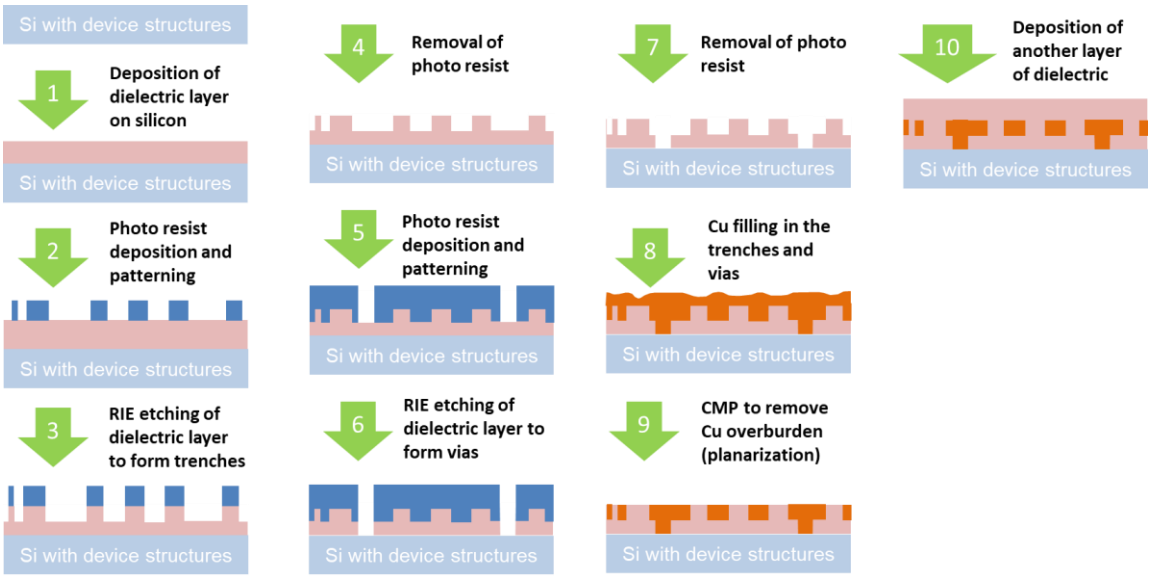

Figure 1.3 Dual-damascene process for BEOL

1.2.2 Package Substrate RDL Processes and Materials

1.2.2.1 Dielectric Materials for Package Substrates

Thicker dielectric layers (15- 40 μm thick) are used in package substrates to insulate the thicker copper wiring (8- 15 μm thick) structures to form coarse pitch I/Os. Thick polymer layers can induce large stresses due to the difference in coefficient of thermal expansion (CTE) between the polymer and copper. Therefore, the polymer resins are filled with inorganic particles to decrease the CTE of the dielectric layers [8]. Typical filler materials used for such build-up films are ceramic materials such as silicon oxides (silica), aluminum oxides (alumina), titanium oxides (titania) and boron nitride. The build-up materials are fabricated as dry films and laminated by vacuum lamination, which simplifies the processing on large panels, eliminating the need to handle solvents.

Additionally, the build-up materials are compatible with electroless plated copper seed layers, leading to high throughput wet chemical processes on large panels at lower cost than BEOL wiring [9].

1.2.2.2 Conductor Wiring Processes for Package Substrates

Copper has been used as a conducting material in package substrates because of its low electrical resistance and high electro-chemical migration resistance. Conductor wiring processes can be classified into subtractive, semi-additive and full-additive processes. The subtractive process is very similar to aluminum RIE patterning for BEOL (Figure 1.2). Instead of aluminum, thick copper is deposited or laminated on the entire surface, then photo resist is patterned on top of the copper layer. Finally, copper chemical etching process is used to form patterned copper structures [10]. The main drawback of the subtractive method is undercut of copper because of the isotropic etching by the chemical etchant (Figure 1.4), which limits the capability of fine structuring to 30 μm and larger.

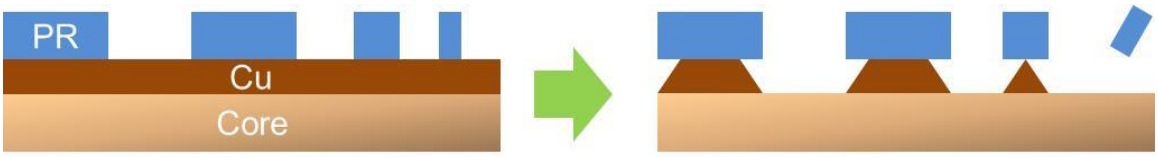

Figure 1.4 Undercut of subtractive process due to side etching (left: before etching, right: after etching)

To address this issue, semi-additive processes (SAP) were developed. SAP begins with electroless copper plating to form an ultra-thin conductive seed layer, followed by

photolithography to pattern the photo resist on the surface. Copper electrolytic plating is then used to form metallization structures between the photo resist patterns, followed by removal of photo resist and micro-etching of the copper seed layer to complete patterning (Figure 1.5). In SAP, side etching can be dramatically reduced compared to the subtractive method because the copper seed layer thickness is much smaller than the thickness of the copper traces [11]. SAP processes have advanced to wiring dimensions down to 10 μm, however, the small amount of side etching during the seed layer removal process has challenged line width scaling below 10 μm.

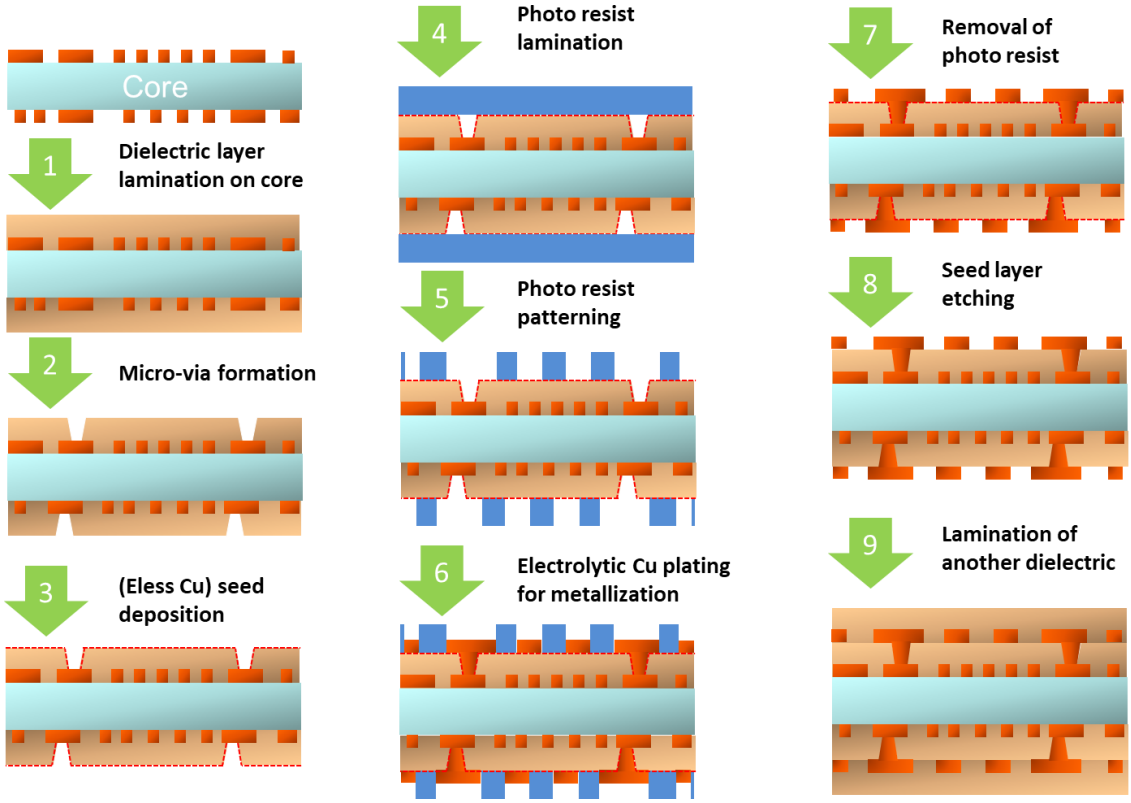

Figure 1.5 Semi-additive process used in package substrates

To eliminate the etching process completely, full-additive processes are being developed. In this process, first, the dielectric surface is catalyzed and photo resist is patterned on the surface. Then electroess copper plating is applied to form copper wiring structures. Finally, the photo resist is removed to complete patterning (Figure 1.6). Wiring can be formed without side etching with fully-additive processes because there is no seed layer to be removed [12]. However, there are challenges in scaling to high volume manufacturing, such as limited availability of photo resist materials that survive highly alkaline electroless copper plating process, very low in process speed of electroless copper plating, and poor mechanical properties of electroless-plated copper due to impurities in the plating bath.

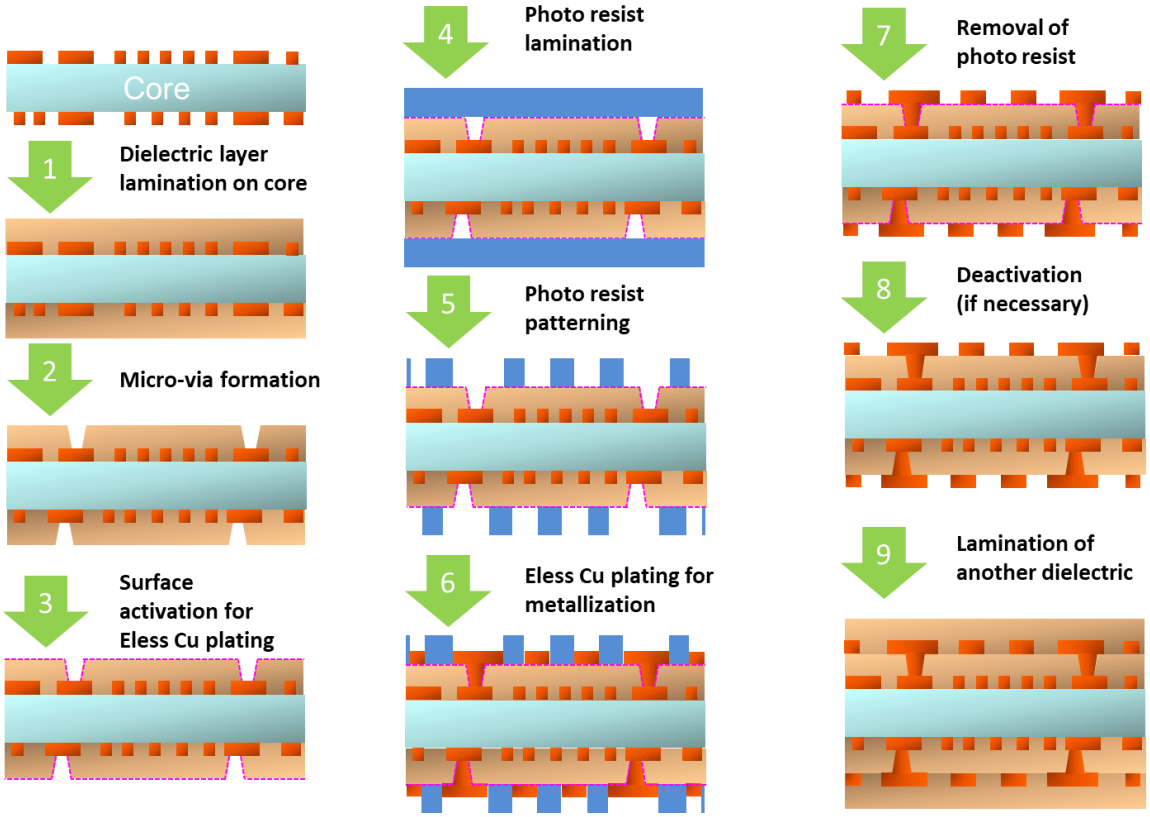

Figure 1.6 Full-additive process for packaging

A recent approach to eliminate the etching process is embedded trench technology. One of the early examples is Via2^{TM} technology developed by Amkor, Atotech and Unimicron [13, 14]. It emulates the dual-damascene process schemes used in the BEOL and replaces SiO_2 dielectrics and RIE etching with polymer dielectrics and excimer laser ablation patterning (Figure 1.7). The embedded trench approach has two main scaling challenges, (a) formation of ultra-small trenches with rectangular profiles, and (b) the removal of the copper overburden after copper filling of trenches and vias by electrolytic plating. In prior work on Via2^{TM} technology, CMP processes adopted from wafer BEOL were used to remove the copper overburden, which limits its application to large panels and increases the process cost significantly. The resolution of the trench width and micro-via diameter made by excimer laser ablation has been limited by traditional dielectric polymers that contain large filler particles for CTE reduction.

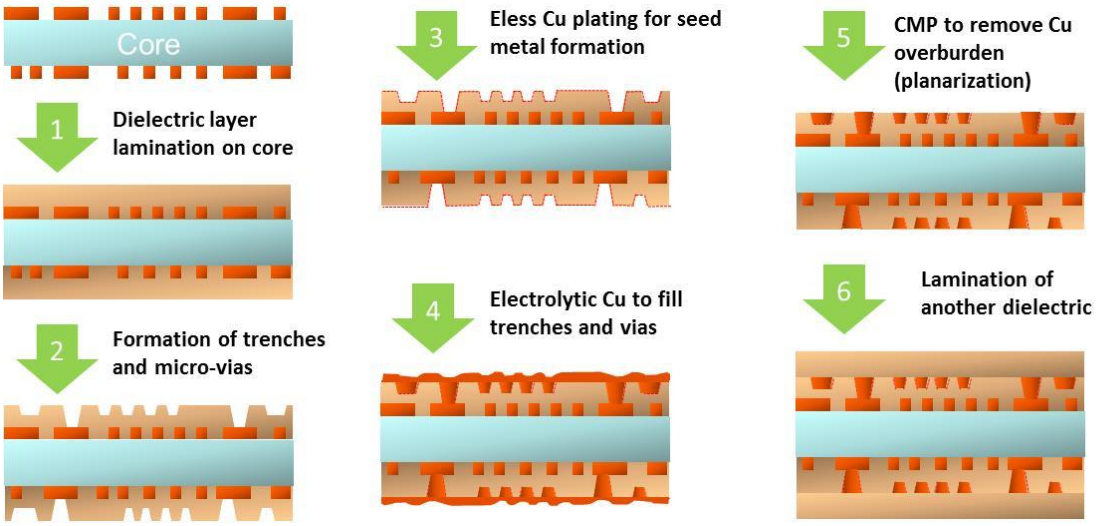

Figure 1.7 Via2^{TM} process for package substrate

1.2.2.3 Micro-via Formation Processes

Four major process methods for the formation of micro-vias in package substrates are described in this sub-section, namely, plasma etching, photo-lithography, conductive paste printing, and laser ablation. Similar to the RIE method in BEOL, plasma etching processes were developed for package substrates such as DYCOstrate technology [15]. In this method, microwave-gas plasma is used to etch the polymer dielectric layers for micro-via formation, while protecting other areas by hard mask materials. The advantage of the plasma etching process is high throughput due to the parallel creation of all the vias at one time. However, the etching process is isotropic, which makes it difficult to form micro-vias below 75 μm diameter. Recently, research teams at ULVAC reported micro-via formations in polymer dielectrics using reactive ion etching (RIE) of direct plasma processes [16]. Due to the anisotropic etching characteristic of RIE process, micro-vias as small as 10 μm diameters were demonstrated. However, throughput and scalability to panel size is limited since the process requires vacuum and voltage bias in processing. Photosensitive dielectrics can also form all micro-vias on a panel or wafer at once by photolithography processes. However, there are some drawbacks, such as limited selection of materials, inferior material properties due to photo chemicals used to achieve sensitivity, and relatively large micro-via sizes (down to 25 μm) in dry film photo materials [17]. Despite recent reports with photosensitive dielectrics to achieve ultra-small micro-via structures below 10 μm [18, 19], such materials have much less or no inorganic fillers to maximize the resolution, which results in high CTE with compromised mechanical reliability. In order to reduce the process time, co-lamination

processes with conductive inks to form micro-vias, such as “any layer inner via hole (ALIVH)” by Panasonic [20] and “buried bump interconnection technology (B^2IT^{TM})” by Toshiba/ DNP [21] were developed. These technologies enabled fabrication of each layer separately and lamination to build multi-layer structures at one time. ALIVH uses prepregs with laser drilled micro-vias filled with copper paste. B^2IT^{TM} uses printed silver paste bump, piercing the laminated prepregs to form micro-via connections. In both cases, paste printing processes limit micro-vias to larger than 50 μm. The most common micro-via process in the manufacturing of package substrates today is CO_2 laser drilling because of the relatively low cost of ownership (CoO) with high throughput. Although CO_2 laser drilling is a serial process and forms micro-vias one by one, the drilling speed is very fast; several thousand vias can be processed in one second. However, due to the long characteristic wavelength (10.2, 10.6 μm) and large beam focus size, formation of micro-vias to less than 30-40 μm is quite challenging. To achieve smaller micro-via sizes, lasers with characteristic wavelength in ultra violet (UV) range have been used. Nd-doped yttrium aluminum garnet (Nd-YAG) laser has a characteristic wavelength at 1064 nm, and the 3rd harmonic wavelength of 355 nm is in the UV spectrum and effectively ablates dielectric layers to form micro-vias with much smaller size. Although the smallest micro-vias with 20 μm diameter were demonstrated using the Nd-YAG UV laser [22], there are some limitations in Nd-YAG UV lasers for further miniaturization. One of the biggest challenges is the positional accuracy of the drilled via locations. Similar to CO_2 lasers, drilling with Nd-YAG UV laser is a sequential process, and the via positional accuracy is defined by the mechanical galvo or stage control, with the best systems achieving ±4 μm accuracy. Furthermore, FR-4 cores made of polymer composites have

poor dimensional stability during thermal processes, which further deteriorates the positional registration of micro-vias. This positional shift requires larger capture pad sizes to guarantee the landing of micro-vias, thus limiting wiring density.

1.2.3 eWLP/ FO-WLP Processes and Materials

In case of eWLP/ FO-WLP, liquid photosensitive polymer dielectric materials are coated on silicon or reconstituted molded wafers. Polyimide (PI) is widely used for its high insulation resistance and high elongation to failure. The high curing temperatures of PI, however, are not compatible with low temperature epoxy molding compounds used in fan-out WLP, and hence polybenzoxazole (PBO) or benzocyclobutene (BCB) dielectrics have been introduced to replace PI dielectrics. Materials used in these processes are liquid photosensitive type and micro-vias with 5-10 μm diameters are formed by photolithography processes. To form conductor structures, PVD Ti-Cu seed is deposited first on the dielectric layer surface, then SAP method is used for patterning. If planarity is needed, CMP is used for planarization of each layer. An extremely flat surface after CMP is essential for high resolution photolithography, and very smooth interface of PVD Ti-Cu seed layer to polymer is preferable to minimize the side-etching during the seed layer removal process. As a result, small wiring structures down to 2 μm can be achieved with SAP for eWLP/ FO-WLP [2].

Recently, organic interposers have been demonstrated by adopting eWLP/ FO-WLP processes to form thin-film RDL on thick polymer-glass composite laminate cores. After the formation of “coarse” RDL layers, the surface of this RDL is planarized with CMP and finer RDL is formed with liquid photosensitive dielectric materials (Figure 1.8)

to achieve 2 μm copper lines and 10 μm micro-vias [23, 24]. However, the fine RDL processes use silicon wafer fab tools, which leads to high cost. Furthermore, poor dimensional stability of organic core materials requires relatively large capture pad sizes for micro-via landing.

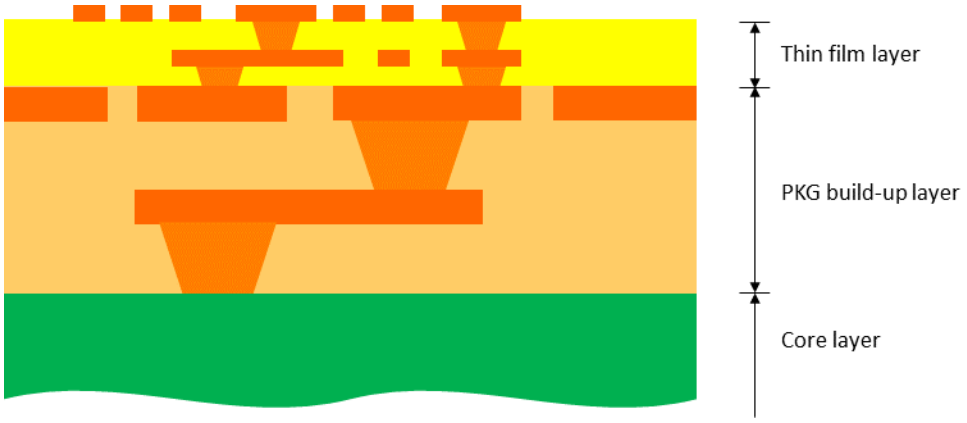

Figure 1.8 Organic interposer using "thin-film" materials and processes.

1.2.4 Summary of Current RDL Materials and Processes

Table 1.1 summarizes the RDL processes and materials used in BEOL, organic package substrates, and eWLP/ FO-WLP

Table 1.1 Summary of the materials and processes in Si BEOL, eWLP/ FO-WLP and build up Package Substrates

		Si- BEOL [25, 26]	Build up package [27-29]	eWLP/ FO-WLP [2, 3]
Dielectric layer	Material	Vapor deposited ceramics (SiO2, F-SiO2, SiOC, TiN, TaN)	Dry film polymer composite (epoxy, LCP)	Liquid polymer (PI, PBO, BCB)
	Process	CVD, HDP	Lamination	Spin coating, Spray
	Thickness	1-3 µm	15-40 µm	5-10 µm
Conductive	Material	Al, Cu	Cu	Cu
	Process	PVD, CVD	Eless plating	PVD
	Thickness	~1 µm	10-25 µm	2-5 µm
Wiring	Process	RIE for Al, (Dual)Damascene for Cu	Subtractive, SAP, Full-additive	SAP
	Width	100 nm	10-25 µm	2-10 µm
Micro-via	Process	RIE (dual-damascene)	CO2 laser, Solid UV laser, Plasma, Photosensitive dielectric, Ink process	Photosensitive dielectric
	Diameter	100 nm	25-50 µm	5-10 µm
Planarization		CMP	Film flow during lamination	CMP

1.3 Limitations of Current Materials and Processes

The 2.5D interposers and other high I/O density packages require scientific and technological advances in ultra-thin insulating dielectric materials as well as in the associated processes to form ultra-small conductors. RDL dielectric film thicknesses scale with pitch, requiring dry films below 6 µm for 20 micron pitch I/Os driven by 50 ohm impedance need. Conductor wiring and micro-via processes need to achieve highly

reliable fine pitch (2 µm lines, <5 µm vias at 20 µm I/O pitch) multilayer RDL with low line resistance conductors at high throughput.

Large panel manufacturing with high throughput RDL processes have been well established with organic package substrates at coarser dimensions, and have been scaling to smaller dimensions in recent years driven by panel fan-out packaging. However, there is a major need for advanced dielectric materials that meet all the required electrical, mechanical, thermal, chemical, and adhesion properties. For example, lower electrical loss is required for high speed signal transmission and low coefficient of thermal expansion (CTE) is required for reliability of multi-layer RDL structures with high aspect ratio. Additionally, the dielectric layers are limited in scaling by available thick dry film polymers (20-30 µm). The main limitation in reducing this film thickness is the use of very high volume percentage of silica or glass microsphere fillers used to reduce the CTE of the dielectric close to that of copper (17 ppm/°C). These thicker films also impose severe limits on reduction of micro-via and trench sizes, since most lasers and dry etching processes have a finite amount of tapering in the via or trench profiles. Furthermore, as the dimension of the wiring and micro-via structures are decreased, such thick dielectric cannot meet the 50 ohm impedance matching for minimal reflection loss of the signal transmission. Moreover, the polymer-glass composite core materials used in the current organic packaging suffer from poor dimensional stability during process temperature excursions, requiring large micro-via capture pads, and thus limiting the ability to achieve fine I/O or bump pitch routing. Silicon interposers by BEOL materials and processes meet the requirement of fine pitch interconnection with high dimensional stability of the silicon substrate. However, they have a fundamental limitation in scaling of RDL

conductor and dielectric thickness higher than 1 μm, which results in large signal loss and RC delay because of high line resistance of thin conductive wiring and high line capacitance of thin dielectric. eWLP/ FO-WLP technologies can accommodate larger dimension than BEOL, however, they have significant limitation in surface planarity due to the conformal nature of liquid coated dielectric materials leading to poor planarity after layer deposition. Liquid polymer materials are coated by spin or spray coating processes. These materials deposit on the underlying copper structures conformally, which requires an additional CMP process to planarize the surface (Figure 1.9). CMP is very effective to planarize but at high cost of consumables such as slurries and polishing pads.

Figure 1.9 Conformal coating of liquid polymer materials

In addition, organic molding compounds used for FO-WLP cause significant dimensional instability, which limits the scaling of the technology to smaller dimensions. To address this issue with positional inaccuracy, “RDL-first” architecture has emerged. In the RDL-first approach, RDL layers are formed first on glass or silicon temporary wafers to secure the positional accuracy, then the temporary wafers are de-bonded and IC chips are embedded on top of the RDL layers with organic molding compounds. Since RDL layers are formed on the inorganic wafers, quite high overlay accuracy can be achieved. However, there are still some challenges such as large warpage after molding and yield loss during carrier bonding and de-bonding process steps.

As discussed, all current RDL materials and processes have challenges in meeting the demand for future 2.5D interposer of high density fan-out packaging. To achieve the goal of this dissertation, new materials and processes to address these challenges need to be explored and demonstrated.

1.4 Novelty of Proposed Research

This research is focused on addressing the limitations of current approaches by; 1) exploring a new generation of ultra-thin dry film polymer dielectric materials with the desired properties and 2) innovative processes to form ultra-small structures to achieve 20 μm I/O pitch multilayer RDL structures on wafers and panels. The unique features of the proposed RDL materials and processes research include (a) design and demonstration of a novel ultra-thin RDL dielectric material that satisfies the properties for RDL with scalability of conductor wiring to 2 μm by SAP, (b) investigation of an innovative embedded trench process with fly-cutting planarization tool to achieve 5 μm diameter micro-vias, and 2 μm wiring traces with high positional accuracy at ±1-2 μm, (Figure 1.10).

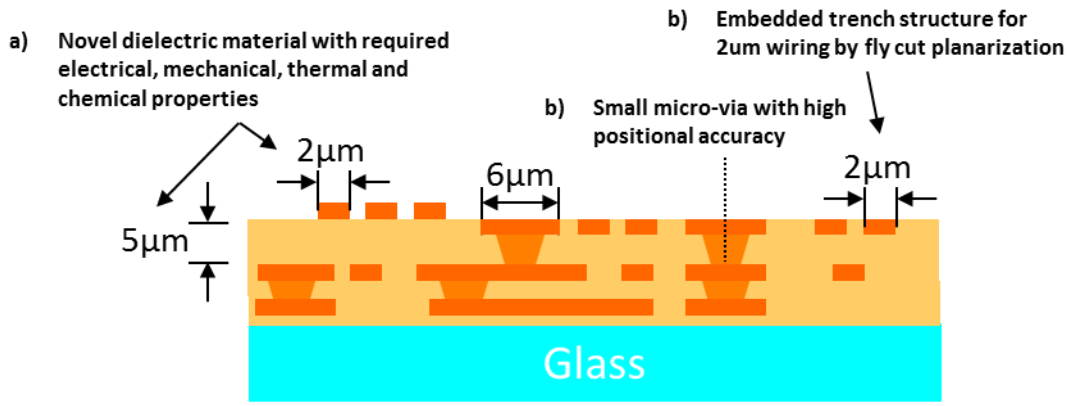

Figure 1.10 Key innovations of the proposed approach

1.5 Fundamental Challenges and Proposed Research Tasks to Address Challenges

To achieve the objectives described in the previous section, there are fundamental challenges to be addressed such as

a. thin film polymer dielectric materials with the required properties
b. small micro-via and conductor line and space processes to form multilayer RDLs at 20 µm I/O pitch

Research tasks to address these challenges are:

a. Design and characterization of ultra-thin dry film polymer dielectric materials with the desired electrical, mechanical, thermal and chemical properties
b. Exploration of innovative embedded trench processes for line and micro-vias

1.6 Thesis Outline

Chapter 1 defines the motivation for the research, specific research objectives, fundamental material and process challenges to achieve these objectives, and research tasks to address the challenges.

Chapter 2 includes a critical literature review of the prior work most relevant to addressing the fundamental challenges defined in Chapter 1.

Chapter 3 describes the design, demonstration and analysis of a dry film material to form ultra-thin polymer dielectric layers with properties required for next generation RDL. Rationale for the requirements will be provided in this chapter. Detail design of the dielectric thickness based on the 50 ohm impedance matching calculation and thermo-mechanical properties based on the finite element modeling approach will be described. Additionally, a new polymer material concept for the advanced polymer dielectric will be introduced and the analysis of the material performance will be conducted. Characterization of the adhesion performance of the new material and analysis of the bonding mechanism will be explored.

Chapter 4 presents the investigation of new process approaches to form embedded trench and small micro-vias using atmospheric ozone etching processes or excimer laser ablation. The in-depth analysis of the effect of filler size on trench profiles is described. Additionally, the impact of metallization processes and core materials will be analyzed and discussed. This chapter also includes multi-layer RLD reliability testing.

Chapter 5 describes summary and contributions of this dissertation.

CHAPTER 2. LITERATURE REVIEW

This chapter reviews the most relevant published literature and recent prior art in addressing the fundamental research challenges identified in Chapter 1. These fundamental challenges are;

c. Ultra-thin film polymer dielectric materials with the required properties
d. Small micro-via and conductor line and space processes to form multilayer RDLs at 20 μm I/O pitch

2.1 Thin Dry Film Dielectric Material

2.1.1 Electrical Properties of Dielectric Materials

One of the most significant application of high density RDL is Wide I/O, which requires 2 Gbps per channel signal transmission. For such high speed signal transmission, signal integrity is one of the critical issues to be addressed. To achieve excellent signal integrity, dielectric losses need to be reduced, which are largely dependent on the polarity (in strength and density) of the polymer molecules [30, 31]. Polymers with extremely low polarity, such as polytetrafluoro ethylene (PTFE) [32] and polysiloxane [33] have ultra-low dielectric loss, and can achieve low loss signal transmission. However, polymers with such low polarity suffer from very weak adhesion at the interface to copper lines due to small van der Waals force, inducing delamination of fine pitch metal wiring structures formed on the polymer surface. Liquid crystalline polymers (LCPs) also have very low

dielectric loss [34], however, high processing temperatures (>280 °C) and poor dimensional stability of the polymer are barriers to its application for fine pitch RDL. Hydrocarbon polymers such as polyolefin [35, 36], polystyrene [37], benzocyclobutene (BCB) [38], and ring-opened norbornen type polymers [39] have quite low polarity and low loss because they are only composed of hydrogen and carbon atoms. Most of the hydrocarbon polymers are thermoplastic, which are not resistant to high temperature solder reflow at 260 °C. Furthermore, these hydrocarbon polymers generally have weak bonding to metal layers, hence they require mechanical roughening or special treatments to enhance adhesion, which poses electrical or reliability issues. Polymer materials are often mixed with ceramic filler components to enhance thermal and mechanical properties such as coefficient of thermal expansion (CTE) and modulus. In such case, selection of low loss filler materials is obviously critical. In addition, the surface chemistry of the filler materials largely affects the loss of composite materials, because small filler particles have large surface areas. A study of epoxy-silica composites, with two different types of silica fillers; fused silica and sol-gel silica, revealed that a composite with sol-gel silica showed a much higher dielectric loss due to the high moisture uptake on the hydrophilic surface [40].

2.1.2 Thermo-mechanical Properties and Reliability of Dielectric Materials

Structural mechanical failure in electrical packages originates as a result of fatigue due to the residual stress from the thermal process excursions. For the evaluation

of the reliability of packages, accelerated tests under thermal cycling are used and the standard procedure is defined by JEDEC [41]. Under the thermal cycling test, cycles to failure (N_f) is described by the Engelmaier's equation as

$$\Delta\varepsilon = N_f^{-0.6} D_f^{0.75} + 0.9 \frac{R_m}{E_{Cu}} \left(\frac{e^{D_f}}{0.36}\right)^{0.1785 \log\left(\frac{10^5}{N_f}\right)} \qquad \textbf{Equation 2-1}$$

where $\Delta\varepsilon$ is the total strain range (TSR), N_f is cycles to failure, D_f is ductility coefficient of the material, R_m is tensile strength of the material, and E_{Cu} is Young's modulus of the material. In most cases, failure of the micro-via occurs in copper at the interface to the polymer dielectric materials. Ramakrishna et al. studied the effect of micro-via geometry on TSR and reliability [42]. They modeled micro-via diameters from 50 μm to 125 μm with varying dielectric thicknesses from 35 μm to 70 μm. The study concluded that as the diameter of the micro-via was decreased for a fixed dielectric thickness, TSR in micro-via increased because of the increasing aspect ratio. Yamanaka et al. reported on the FEM modeling of the impact of material properties and geometry on thermo-mechanical strain in the micro-via [43]. In this report, micro-via diameters from 20 μm to 30 μm and heights from 10 μm to 60 μm were varied and the influence on micro-via TSR was calculated. It was concluded that the most dominant factor was the aspect ratio of the micro-via. As the aspect ratio increased, thermo-mechanical strain in copper at the interface increased (Figure 2.1). They also calculated the strain with a fixed aspect ratio while changing the scale factor. It was observed that shrinking the entire dimension (x, y and z) of the system led to a reduction in strain in the micro-via. This result encourages the scaling down of the micro-via structure by reducing the dielectric layer thickness and the micro-via diameter. This research provided a positive guideline

for miniaturization of the micro-via dimensions. However, no detailed analysis was conducted for micro-via diameter and polymer dielectric layer thickness less than 10 μm.

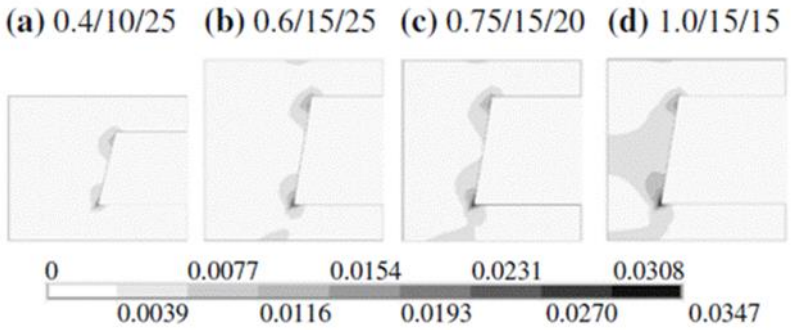

Figure 2.1 Effect of aspect ratio on via strain [43]

For the assessment of small micro-vias below 10 μm, Filippi et al. studied the stacked micro-via reliability in RDL made by BEOL processes [44]. In this paper, statistical analysis of small micro-vias revealed that the cycles to failure in copper have a strong dependency on the temperature range of the thermal cycle test. However, the impact of micro-via geometry was not discussed in this research.

Another factor to define the TSR in micro-vias are the properties of the dielectric material. Lesniewski analyzed the effect of dielectric material properties on micro-via reliability through empirical investigations [45]. In this work, reliability tests were conducted with several materials with different CTE values. The cycles to failure increased as the CTE of the polymer dielectric was reduced from 70 ppm to 38 ppm. Mahalingam et al. worked on FEM modeling to assess the impact of dielectric material properties [46]. After the independent calculation of the residual strain by varying some

of material properties, it was found that the most dominant parameters related to stress and TSR are the modulus and CTE of the dielectric material (Figure 2.2). However, these studies did not consider the inter-relationship between the modulus and CTE of a material, which is defined by the fraction of filler content in the dielectric.

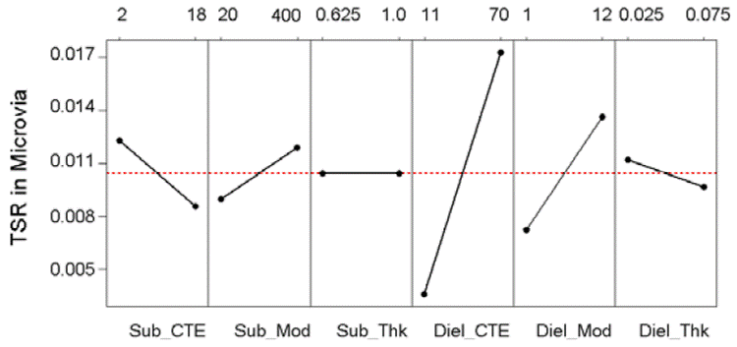

Figure 2.2 Effect of material properties on strain in micro-via [46]

2.1.3 Adhesion Properties

Strong adhesion between copper metallization and the polymer dielectric layer is critical for multi-layer RDL with high thermo-mechanical reliability. Surface roughening in the order of sub-micron to micron by desmear processes are applied to dielectric layers before seed copper deposition by electroless Cu plating, in order to enhance the interfacial bond strength. However, such micron-scale roughness imposes additional challenges of higher side etching during seed layer removal, impacting the line width control for fine lines, and the interfacial roughness also increases electrical transmission loss due to the skin effect, especially at higher frequencies. This subsection describes the previous studies on lowering surface roughness of polymer dielectric materials, while

attempting to achieve high interfacial bond strength. Sun et al. researched the correlation between the roughness of an epoxy-silica composite film dielectric induced by desmear process and adhesion to copper metallization [47]. It was observed that lower desmear process time resulted in lower surface roughness and weaker peel strength of the copper metallization. Therefore, simply reducing the desmear process time to achieve smoother interfaces only leads to the delamination of plated copper due to weak bonding. As an alternative to wet chemical treatment, surface roughening by plasma treatment was also reported. Venkatesh et al. used fluorine containing gas such as CF_4 and C_2F_6 to increase the adhesion between polymer and metal by etching polymer to roughen the surface [48]. However, both wet and dry roughening approaches in the published literature have required micron scale roughness to achieve sufficient metal to polymer bonding strength.

Various process approaches have been reported to increase adhesion of polymer dielectric without micron-scale roughening. The first category is the chemical modification of the polymer surface. Sugimoto et al. reported on enhanced adhesion of deposited metal to the polymer surface by UV irradiation [49]. UV irradiation of the polymer surface induced the creation of activated chemical groups such as –OH, -C=O, and -COO. These highly polar chemical groups can enhance the adhesion between the polymers and surface metallization. A plasma treatment with NF_3 gas was also reported to enhance the surface adhesion by incorporation of –C=N group into the polymer surface [50]. Additionally, chemical deposition of bonding agent such as organometals, amines, and silane coupling agents was reported to be effective to increase bonding processes [51, 52]. However, adhesion with these chemical modification processes tended to decrease after highly accelerated stress tests (HAST) under high temperature and high moisture

conditions because of the degradation of the chemical bonding by moisture absorption. The second category, is the deposition of bonding agents on the polymer surface. Surface treated silica nano particles with silane bonding agent effectively increased bonding strength between polymer surface and metallization [53]. Improved bonding by surface polymer grafting was reported by selecting proper graft polymer units [54, 55]. However, these additional surface layers can cause issues at micro-via connections, resulting in high electrical resistance or open failures (Figure 2.3) [56].

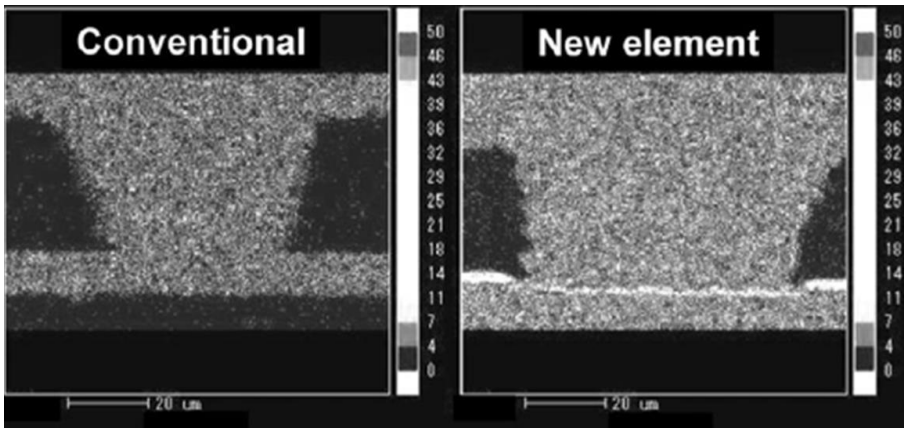

Figure 2.3 Residue of the newly applied element on the bottom of micro-via [56].

2.2 Small Micro-via and Copper Wiring Processes

2.2.1 Traditional Micro-via Processes

Micro-via formation processes can be classified into (a) parallel (multiple vias formed at the same time) and (b) serial (vias formed one at a time) approaches. There are several parallel via formation methods explored in the prior art, with a focus on higher process throughput by forming a large number of vias at the same time, primarily based

on plasma etching, photo-lithographic techniques or conductive paste printing. In the silicon wafer BEOL, dual-damascene processes using reactive ion etching (RIE) can form sub-micron micro-vias. Micro-via formation in polymer dielectrics using RIE of direct plasma processes was reported for high density packaging applications [16]. Due to the anisotropic etching characteristic of RIE processes, the size of the micro-vias are only dependent on the mask opening size. Hence, ultra-small size micro-vias below 1 μm can be fabricated. However, process speed is quite limited since the processes require high vacuum and voltage bias. Isotropic plasma etching processes were developed such as DYCOstrate technology [15] with high processing speed due to the parallel creation of all the vias at one time. However, large side etching by isotropic etching makes it difficult to form micro-vias below 75 μm diameter. Photosensitive dielectrics can also form 25 μm micro-vias in the entire panel simultaneously by photolithographic processes [57]. Recent progress in the development of next generation photosensitive dielectric materials enabled micro-via formation down to 5 μm [58]. However, these materials are not proven to be fully reliable in packaging applications because there are some drawbacks of photosensitive dielectrics, such as inferior material properties due to photo sensitivity, and reduced amount of filler incorporation for optical resolution. In order to reduce the process time, co-lamination processes with conductive inks to form micro-vias, such as "any layer inner via hole (ALIVH)" by Panasonic [20] and "buried bump interconnection technology (B^2IT^{TM})" by Toshiba/DNP [21] were developed. These technologies enabled the fabrication of each layer separately and lamination to build multi-layer structures all at once. ALIVH uses prepregs with laser drilled micro-vias filled with a copper paste. B^2IT^{TM} utilizes a printed silver paste bump, piercing the laminated prepregs to form

micro-via connections. In both cases, paste printing processes limit the capability of micro-via formation at less than 50 μm.

The second category involves forming one via at a time using so-called "serial" processes. The most common such micro-via process for package substrates today is CO_2 laser drilling, because the drilling speed of a CO_2 laser is very fast; several thousand vias can be processed in one second. However, due to the long characteristic wavelength (10.2, 10.6 μm) and large beam focus size, formation of micro-vias less than 30-40 μm is challenging [59]. To achieve smaller micro-via sizes, lasers with characteristic wavelengths in the ultra violet (UV) range have been used. 355 nm Nd-doped yttrium aluminum garnet (Nd-YAG) lasers effectively ablate polymers to form micro-vias with much smaller size down to 20 μm [22]. There are some limitations in Nd-YAG UV lasers for further miniaturization. One of the biggest challenges is the positional accuracy of the drilled vias. Similar to the CO_2 laser, drilling processes of Nd-YAG UV lasers are sequential, which limits the positional accuracy, defined by the mechanical galvo or stage control (±4 μm). The positional shift requires larger sized capture pads to guarantee the proper landing of micro-vias. Table 2.1 summarizes the various micro-via formation methods in epoxy-based dry film materials.

Table 2.1 Micro-via formation in epoxy film materials through various methods

Method	Via ϕ (μm)	Depth (μm)	Serial/ Projection	Drawback
CO2 laser [59]	65	40	Serial	Large via size Positional instability
Nd-YAG laser [60]	25	35	Serial	Positional instability
Paste printing [22]	50	50	Serial	Large via size
Isotropic Plasma [61]	75	50	Projection	Large via size
Anisotropic Plasma [16]	10	5	Projection	Low throughput
Photosensitive [57]	5	10	Projection	Limited material selection Stress by large CTE

2.2.2 Emerging Via Formation Methods: Excimer Laser Ablation

To achieve high registration accuracy and small micro-via formation, mask projection laser process by excimer laser ablation has a significant advantage, since it has very large beam focus. The cross section of the excimer beam has a rectangular beam shape at high power, reflecting the shape of the discharge area. Due to the large pulse energy of the excimer laser beam, it is suitable for applications that process large areas with mask projection. Utilizing this character of the excimer laser, preliminary research on micro-via formation with excimer lasers have been conducted in filler-less polymer materials, such as Polyimide and BCB [48, 62, 63]. Some of the early work also reported that the excimer laser was able to form micro-vias in epoxy-silica composite materials [64]. However, there is no analysis regarding the registration accuracy of the micro-vias on the capture pad, and limited published work on small micro-vias in ultra-thin polymer dry films and their reliability.

2.2.3 Cu Wiring Processes by Semi-additive Process (SAP)

SAP processes have been advancing to wiring dimensions down to 10 μm by dramatic reduction of side etching compared to the subtractive processes [11]. Recently, organic substrates with SAP RDL have been demonstrated down to 5 μm line and space through process optimization [20-22]. However, SAP methods face challenges in scaling below 5 μm, primarily limited by the side etching of the copper lines during seed layer removal, and poor adhesion of ultra-fine lines on smooth dielectric surfaces. By using liquid dielectrics and sputtered Ti-Cu seed layer, ultra-small line formation down to 2 μm with SAP was demonstrated [23, 24]. However, liquid dielectrics require wafer processes for coating thin layers and sputtered Ti-Cu seed processes require a long pre-bake step under high vacuum, thus limiting high throughput multi-layer RDL fabrication.

2.2.4 Embedded Trench Technology

As an alternative wiring process to SAP, embedded trench technology has been intensively researched and developed in recent years. It emulates the dual-damascene process schemes used in wafer back-end-of-line (BEOL), and replaces SiO_2 dielectrics with polymer dielectrics, and alternates RIE etching by massive parallel trench and micro-via patterning processes, such as excimer laser ablation and photolithographic patterning. The photolithography trench formation methods can achieve small feature sizes down to 1.5 μm due to high resolution of the state-of-the-art photo-sensitive dielectric materials [18, 65, 66]. However, these photo-sensitive materials require very specific catalysts introduced in the polymer matrix to achieve high resolution, and this

impacts the material properties negatively. Based on the focus of designing ultra-thin dielectric material with ideal properties from first principles in this thesis, such methods were not considered for investigation. Therefore, the primary focus of this dissertation research is on massively parallel patterning of ultra-small trenches and micro-vias in ultra-thin non-photo dry film polymer dielectrics. The advantages of such embedded trench approaches with parallel patterning processes compared to SAP are: a. higher aspect ratio line capability, b. elimination of seed layer removal process step, c. ability to pattern lines and micro-vias at the same time, d. reduced number of process steps by eliminating photo lithography processes, and e. via pattern integrity. One of the initial demonstrations of embedded trench processes in dielectric materials was the Via2^{TM} technology developed by Amkor, Atotech and Unimicron using excimer laser ablation [13, 14]. In the initial reports, copper wiring formation down to 13 μm was demonstrated. Although it was mentioned that the inclusion of large filler in the traditional dielectric polymers was one of the limiting factors for further miniaturization of trench size, no detailed discussion of the mechanism was described. A lot of research on trench and micro-via formation with excimer lasers has been conducted and ultra-small trench and micro-via formation below 10 μm was achieved in filler-less polymer materials, such as polyimide and benzocyclobutene (BCB) [48, 62, 63]. A recent study by Unimicron reported the successful trench formation down to 3 μm lines and spaces in a build-up dielectric material with small sized filler [67]. These prior reports highlight the advantage of filler-less or small sized filler inclusion in the trench miniaturization, however, no detailed and fundamental analysis has been conducted on the impact of fillers in the dielectric materials on the laser processes.

2.2.5 Copper overburden removal

One of the main challenges of the embedded trench approach is the removal of the copper overburden after the copper filling of trenches and vias by electrolytic plating. Etching back to remove copper overburden with wet chemical, such as $FeCl_3$ and $CuCl_2$, is the simplest and the most conventional methods, however, control of the etching speed over the entire panel is extremely challenging especially when the feature sizes are small. As a result, etching processes cause damages to small trench and micro-via structures. There are some reports on plasma-based copper etching processes [68, 69], however, such dry etching processes have extremely slow process speed. In prior work on Via2^{TM} technology, CMP processes adopted from wafer BEOL were used to remove the copper overburden, which increases the process cost significantly.

CHAPTER 3. MODELING, DESIGN AND CHARACTERIZATION OF ULTRA-THIN DRY FILM POLYMER DIELECTRIC MATERIALS FOR HIGH DENSITY RDL

This chapter describes the fundamental research into the design and characterization of new polymer dielectric materials as ultra-thin dry films for silicon-like high density RDL on large panels. Thin polymer dielectric layers are critical for high density RDL for several reasons. The first reason is the reduction of the micro-via size, while maintaining a reasonable aspect ratio of via diameter to film thickness. One of the limiting factors for small via formation in dry film polymer dielectric layers, is the thickness of traditional build-up materials (25-30 μm thick). Thicker films require micro-vias with higher aspect ratios for any given via diameter, and the higher aspect ratio presents a number of challenges in high yield and high throughput via formation, as well as the high reliability of micro-via structures. The second reason for ultra-thin dielectric materials is impedance matching of the electrical transmission lines. To minimize the return loss of the transmission line, impedance matching is very important. A thinner dielectric layer is required to design for 50 ohm impedance as the transmission line width decreases. Although liquid polymer dielectric materials can form thin layers, they face planarization challenges due to their conformal coating on non-flat surfaces, Furthermore, liquid materials need wafer processes to form thin layers, which limits high throughput RDL fabrication. Highly planar dielectric surfaces are imperative for ultra-small circuit

formation for multilayer RDL wiring structures. These are the drivers for the exploration of a new class of thin dry film polymer dielectric materials.

In this research, the design and demonstration of an ultra-thin dry film dielectric material, with a set of target properties selected by design from first principles, will be conducted based on modeling and experimental analysis. This chapter begins with the design of a material to achieve the required electrical, thermal and adhesive properties. Electrical design was based on 50 ohm impedance calculations and high speed signal transmission loss, and thermo-mechanical design was based on the finite element modeling (FEM) to ensure lowest stress in the RDL structure. Then norbornene type polymer (NP) based new materials for meeting the required properties will be introduced, followed by the characterization of the electrical and thermo-mechanical properties of the new polymer material and in depth analysis of the properties. Lastly, the adhesion evaluation of the material will be discussed and the bonding mechanisms will be analyzed.

3.1 Target Properties for Thin Dry film Dielectric Materials

An ideal thin film dielectric material for next generation package RDL must meet the following targets for properties and processability to form structures.

- Electrical properties
    - Low dielectric constant and low dielectric loss for the transmission of high speed electrical signals.
    - Ultra-thin film with total thickness variation (TTV) below 5% of film thickness, to maintain 50 ohm impedance

- Thermal properties
    - Low coefficient of thermal expansion (CTE) for lower stress in packages during thermal cycles.
    - Thermal resistance to multiple solder reflows at 260 °C.
- Mechanical properties
    - Low modulus (high compliance) to buffer the stresses arising from CTE mismatch between copper, low CTE core and silicon chips in packages.
    - High elongation to break to reduce the risk of polymer cracking under stress from thermal cycling
- Adhesion properties
    - Strong bonding to copper for better reliability and fine pitch wiring processability.
- Processability
    - Partially cured (B-stage) dry film material with high flow during the lamination process to planarize the polymer surface
    - Excellent chemical inertness and thermal resistance after curing
    - Compatibility to electroless (Eless) copper plating processes to accommodate high speed and high throughput metallization capability

Table 3.1 summarizes the properties of current RDL dielectric materials and the required properties for next generation RDL materials. Build-up film dielectric materials used for current package substrates are polymer-inorganic composite dry film materials based on the epoxy resins and silica fillers. Typical thickness of these materials is in the 20-40 μm range, suitable for the impedance matching to conductive wiring with 15-20 μm width and height. The required properties for the next generation RDL materials are based on the material design described in the following section 3.2.

Table 3.1 Dielectric material properties for current RDL and next generation RDL

Parameters			Current Build-up	Next Gen RDL	Reason
Material Properties	Electrical	Thickness	20-40μm	3-6μm	50ohm impedance matching to 2μm conductor wiring
		Dk	3.0	< 3.0	Low capacitance
		Df	0.018	< 0.010	High speed signal transmission
	Mechanical	Modulus	< 10GPa	< 10GPa	Minimal stress
	Thermal	CTE	45ppm/°C	32ppm/°C	Reduction of stress in RDL
	Adhesion	Peel strength	0.6N/m	0.6N/m	Strong bonding of fine wiring
		Surface roughness (Rz)	> 3μm	< 0.7μm	Reduction of side etching

3.2 Design of the Dielectric Material for Next Generation RDL

3.2.1 Electrical Design 1 - Dielectric Thickness Based on Impedance Matching

As discussed, the thickness of the dielectric material needs to be reduced as the dimensions of conductive wiring get smaller to keep the impedance matching to Z_0. In the case of micro-strip line in package substrates, Z_0 of 50 ohms is generally used. Figure 3.1 shows the configuration of the micro-strip line for the impedance calculation using the equation 3-1. Here, W is the width of copper trace, t is the height of copper trace, H is the thickness of the dielectric layer, Z_0 is the impedance (50 ohm), and ε_r is the permittivity (dielectric constant) of the dielectric. Permittivity of the most of major polymer materials are in the range of 2.1 to 4.2, and many of them have values close to 3.0, therefore ε_r =3.0 was assumed for the calculation.

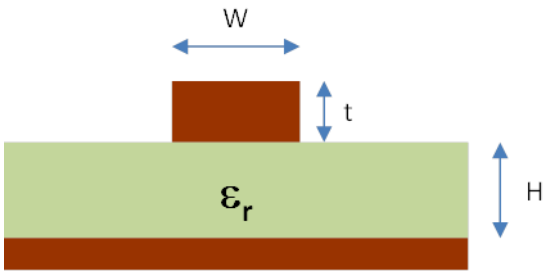

Figure 3.1 Micro-strip line configuration for impedance calculation

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} \ln\left(\frac{8H}{W_e} + \frac{W_e}{4H}\right)$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left\{\left(1 + 12\frac{H}{W_e}\right)^{-0.5} + 0.04\left(1 - \frac{W_e}{H}\right)^2\right\}$$

Equation 3-1

Here,

$$W_e = W + \frac{t}{\pi}\left(1 + \ln\left(\frac{2H}{t}\right)\right) \ldots \frac{W}{H} \geq \frac{1}{2\pi}$$

$$W_e = W + \frac{t}{\pi}\left(1 + \ln\left(\frac{4\pi W}{t}\right)\right) \ldots \frac{W}{H} \leq \frac{1}{2\pi}$$

Figure 3.2 shows the calculated dielectric thickness with respect to different line width and line thickness (height) to maintain 50 ohm impedance. The plots in the red circle indicate the required dielectric thickness for the 2 μm width wiring. The required thickness of the dry film dielectric materials can be calculated by the sum of the thickness of dielectric layer between the two metal layers and the height of the conductor layer under the dielectric. Therefore, the target thickness of dielectric materials to achieve 50 ohm impedance matching for 2 μm line width is 3 μm for a conductor thickness (t) of 2 μm, and 6 μm for a conductor thickness (t) of 4 μm.

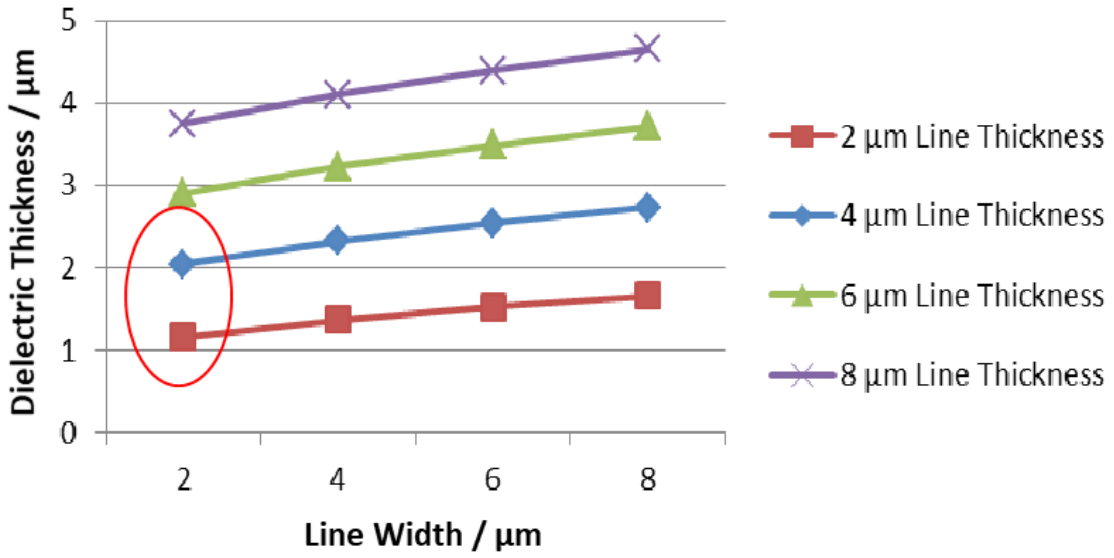

Figure 3.2 Dielectric thickness with various line width and height for 50 ohm impedance matching in micro-strip line configuration

3.2.2 Electrical Design 2 – Dielectric Loss

3.2.2.1 Signal Transmission

For high speed digital application, signal integrity is one of the most important requirements. Digital signals have both a low frequency component and a high frequency component, and both these components need to be transmitted to maintain good signal integrity. However, the higher frequency component tends to decay faster (low pass filter effect) due to higher signal loss at higher frequency. Such a low pass filter effect causes the deterministic jitter and rise-time losses, which reduces the eye opening to deteriorate the digital signals (Figure 3.3). Although a low pass filter effect can be compensated by

the use of passive equalizers [70], the use of equalizers result in larger package size and higher cost and complexity.

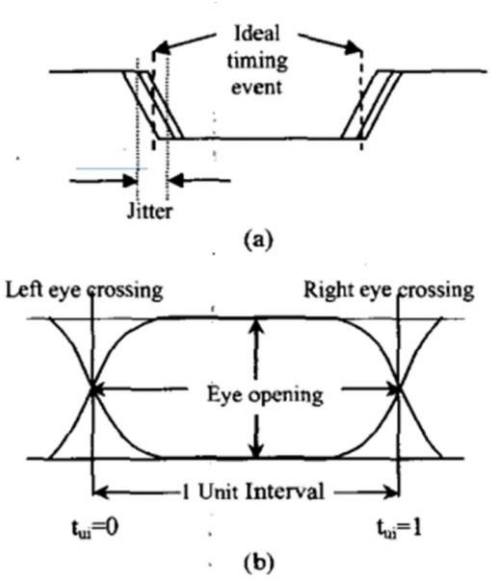

Figure 3.3 Jitter and eye diagram [71]

Signal loss in RDL wiring arises from three major sources; conductor loss, dielectric loss and radiation loss. Conductor loss is dominant when the frequency is relatively low (up to 1-10 GHz) [72], but as the frequency increases, dielectric loss becomes dominant because conductor loss is proportional to the square root of frequency, whereas dielectric loss is directly proportional to the frequency. Therefore, the use of dielectric materials with lower dielectric loss/ dissipation factor (Df) is essential to achieve excellent signal integrity at higher frequencies. For the next generation RDL used for wide I/O applications, signal transmission rate needs to be doubled (2Gbps) to accommodate the requirement of higher bandwidth, resulting in the need for lower loss dielectrics at higher

frequencies. Hence, there is a critical need to reduce the dielectric loss of the current build-up dielectric materials by a factor of 2×, from the current Df of 0.018, to less than 0.009 – 0.010 for the next generation dielectric materials.

3.2.3 Thermo-Mechanical Design

Fatigue failure is a major cause of mechanical failures in electronic packages and in RDL layers due to the ductile copper wiring. Fatigue in metals happens due to cyclic stress/strain induced by CTE mismatch to the dielectric during the thermal excursions. The typical reliability criteria for package substrate applications is no low-cycle fatigue up to 1000 thermal cycles between -55 °C and 125 °C [41]. This fatigue criteria can be converted into the total strain range (TSR) in the package using the Coffin-Manson or derived the Engelmaier equations. In this design, the Engelmaier equation was selected to understand the impact of plastic strain on RDL reliability (equation 3-2).

$$\Delta\boldsymbol{\varepsilon} = \boldsymbol{N_f^{-0.6} D_f^{0.75}} + \mathbf{0.9}\,\frac{\boldsymbol{R_m}}{\boldsymbol{E_{Cu}}}\left(\frac{\boldsymbol{e^{D_f}}}{\mathbf{0.36}}\right)^{\mathbf{0.1785\log\left(\frac{10^5}{N_f}\right)}} \qquad \textbf{Equation 3-2}$$

Material properties of copper were input into the calculation, since cracks in copper generate electrical failures and the highest strain is typically concentrated in copper at the via bottom [43]. In the equation 3-2, $\Delta\varepsilon$ is the total strain range (TSR), N_f is the number of cycles to failure, D_f (=0.302) is the ductility coefficient of copper, R_m (=400 MPa) is the tensile strength of copper, and E_{Cu} (=117 GPa) is the Young's modulus of copper. Figure 3.4 shows the calculated relationship between the number of cycles to failure and the total strain range (TSR) in copper. From this calculation, the total strain range should be below 1.14×10^{-2} to achieve fatigue life above 1000 cycles. Considering a safety factor

of 5×, a total strain range below 6.64×10^{-3} is desirable to achieve fatigue life more than 5000 cycles.

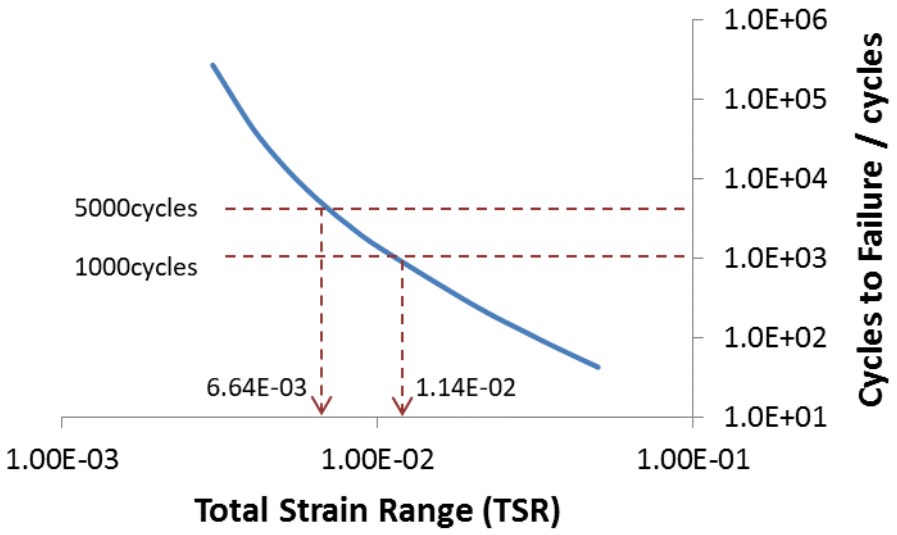

Figure 3.4 Relationship between the TSR and cycles to failure calculated by the Engelmaier's equation

Since the stress or strain in the package comes from the mismatch in the material properties, it is important to design materials to minimize the stress/strain. Among the many material properties, it was reported that coefficient of thermal expansion (CTE) and Young's modulus of the component materials are the most critical parameters for reducing the stress/strain in packages [46]. Especially, large CTE mismatch between the polymers (typically 60-70 ppm/°C) and copper (16.7ppm/°C) or silicon (2.6ppm/°C) is a major source of stress and strain. Pristine polymer materials can be mixed with low CTE inorganic fillers to form composites to reduce their CTE. Such filler materials should have low CTE and high electrical insulation, therefore metal oxides or nitrides are widely

used as filler materials. The typical CTE of different filler materials are; silica: 0.55 ppm/°C, titania: 8.4 ppm/°C, alumina: 7.2 ppm/°C, and boron nitride: 3.8 ppm/°C. Since silica has the lowest CTE, it is widely used as the filler material of choice in dielectric composite materials. Any increase in the inorganic filler content changes not only the CTE of the composite, but also the modulus of these composite materials [42]. Typically, higher filler content results in lower CTE and higher modulus. The lower CTE has a positive impact on stress reduction, whereas the higher modulus has a negative influence. Therefore, it is important to take the combined effect of CTE and modulus into the account for the dielectric material design. Wong has researched the correlation between the fraction of filler volume and CTE of the composite material. In this research, various theoretical models were compared with the experimental results and it was concluded that the predictions by the rule of mixtures and Schapery's upper limit best described the behavior [8]. The rule that describes the mixture is shown in equation 3-3

$$\alpha_c = \alpha_f \phi_f + \alpha_p \phi_p \qquad \textbf{Equation 3-3}$$

where α_c is the CTE of the composite, α_f, ϕ_f are the CTE and the fraction of the filler respectively, α_p is the CTE of the polymer and $\phi_p = 1 - \phi_f$ is the fraction of the polymer.

In case of the modulus, the rule of mixtures does not give good matching to the modulus of the composite. Hurley reported that it can be well described under the Halpin-Tsai equation for a silica-polymer composite [73]. Halpin-Tsai equation is an empirical equation using a fitting parameter ε, and the relationship between the filler content and modulus of the silica-polymer composite material can be described by the equation 3-4.

$$E_c = E_p (1+\varepsilon\eta\phi_f)/(1- \eta\phi_f) \qquad \textbf{Equation 3-4}$$

where E_c, E_p are the modulus of the composite and polymer respectively, ϕ_f is the fraction of the filler, ε is a geometric factor related to the shape of the filler and $\varepsilon=2$ in case of spherical filler, and η is a constant calculated by $\eta = (E_f/E_p - 1) / (E_f/E_p + \varepsilon)$.

These equations were used for modeling to estimate the CTE and modulus of the composite dielectric material. Table 3.2 summarizes the CTE and modulus of the silica-polymer composite with various filler volume fractions. The CTE of most pristine polymer materials ranges from 50 ppm/°C to 70 ppm/°C, and their Young's modulus ranges from 2.0 GPa to 4.0 GPa. Therefore, a CTE value of 60 ppm/°C and a Young's modulus of 3.0 GPa were assumed for the pristine polymer in this calculation. The other input values were α_p = 60 ppm/°C, α_f = 0.55 ppm/°C, E_p = 3.0 GPa, E_f = 70 GPa

Table 3.2 CTE and Young's modulus of the silica-polymer composite material with various filler fractions

ϕf	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
αc (ppm/°C)	60.0	54.1	48.1	42.2	36.2	30.3	24.3	18.4	12.4	6.5	0.6
Ec (GPa)	3.0	3.2	3.7	4.2	5.0	6.1	7.9	10.8	16.7	34.6	70.0

To investigate the effect of these properties on the reliability of stacked micro-vias and to provide a design guideline for material, 3D finite element modeling (FEM) analysis with ANSYS mechanical APDL was conducted. The configuration of the one-eighth symmetric model of the three stacked micro-via and wiring layers is illustrated in Figure 3.5, which has a 100 μm thick glass core, a 10 μm thick buffer layer, 10 μm thick build-up dielectric layers, 5 μm height and 6 μm diameter copper capture pads, 5 μm height and 2 μm width wiring, and 5 μm height and 5 μm diameter micro-vias. To

minimize the calculation time while having more accurate modeling results, a global-local modeling technique in xy direction was utilized with 10 μm × 10 μm × 90 μm rectangular solid for the local model and the 1000 μm × 1000 μm × 90 μm rectangular solid for the global model.

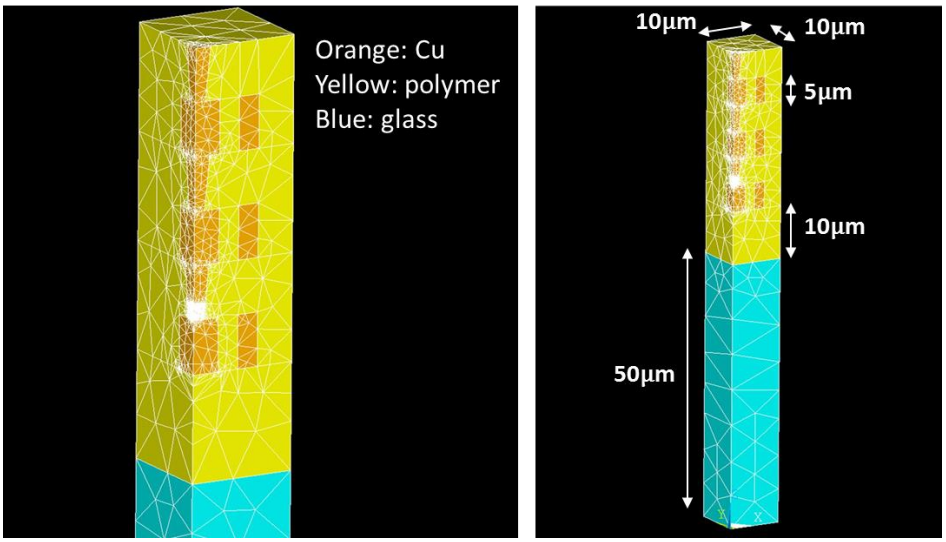

Figure 3.5 Configuration of the stacked micro-via package for FEM analysis (blue: glass, yellow: polymer dielectric, orange: copper)

First, temperature cycling between -55 °C and 125 °C for 3 cycles was applied to the model. Then, the total strain range (TSR) during the thermal cycle was calculated by changing the input material parameters (CTE and modulus in Table 3.2) based on the filler content of the dielectric layers. For the calculation of the TSR, meshed copper elements at the bottom of the micro-via were selected, since this location has the highest strain range, making the region most likely to fail (white circles in Figure 3.6). Singular points at the sharp corners of the micro-via were excluded from the calculation.

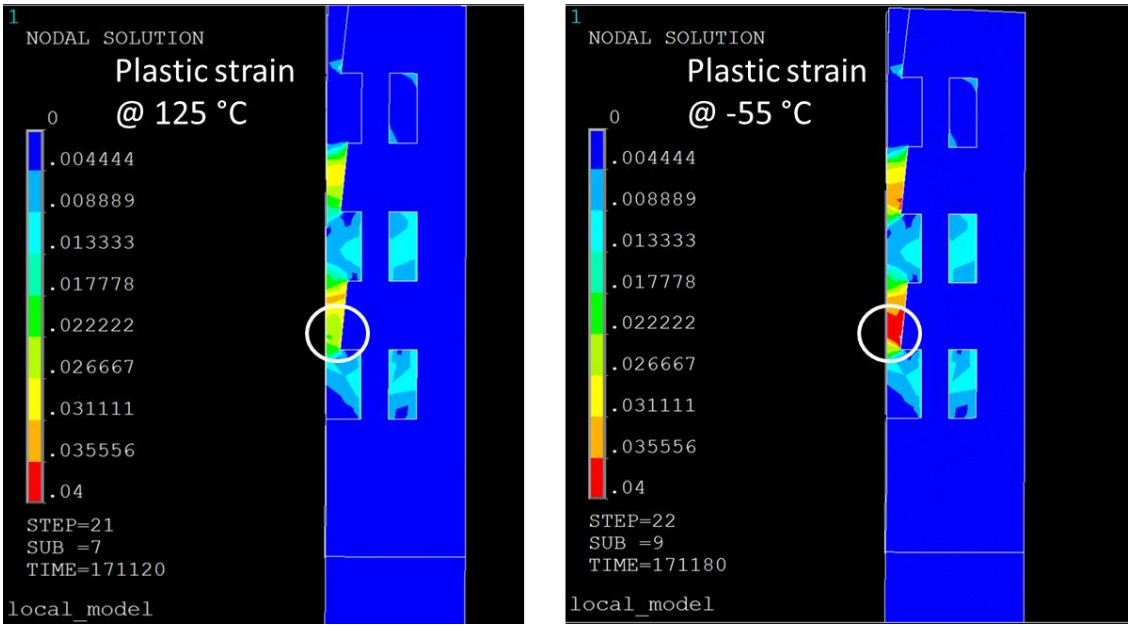

Figure 3.6 Plastic strain in Cu at 125 °C and -55 °C and the location of the elements used for the TSR calculation

Figure 3.7 summarizes the graphs of TSR vs. filler content in the dielectric layer. TSR was reduced by the addition of filler into pristine polymer matrix due to reduced CTE up to the filler content of 0.7. Continuous decrease in TSR in this region implied that the effect of higher dielectric modulus up to 10 GPa with larger filler content was negligible compared to the dramatic reduction of TSR due to lower dielectric CTE. The lowest TSR was observed at the filler content of 0.7, where the CTE of the dielectric material was the closest to the CTE of copper (16.7 ppm/°C). At the range where filler content is larger than 0.7, slight increase in TSR was observed due to small increase in CTE mismatch between the dielectrics and copper, and higher modulus of the dielectric materials. However, the increase in TSR was trivial, and TSR was maintained below 2.0×10^{-3} for the region. To achieve TSR smaller than 1.14×10^{-2} (1000 cycles to failure), filler content

needs to be larger than 0.31, which results in a CTE of the material of less than 41 ppm/°C. For the conservative condition to achieve TSR smaller than 6.64×10^{-3} (5000 cycles to failure), filler content needs to be larger than 0.47, which results in a CTE of the material smaller than 32 ppm/°C.

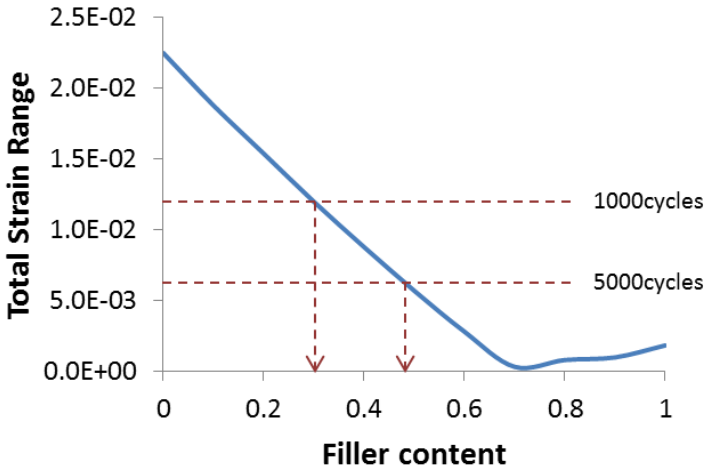

Figure 3.7 TSR in Cu at the via bottom vs. filler content in the polymer dielectric

3.2.4 Design for High Adhesion Strength

Strong adhesion between copper metallization and the dielectric layer is critical for multi-layer RDL with high thermo-mechanical reliability. To have strong bonding at the interface, surface roughening of the order of sub-micron to few microns by desmear processes is usually applied to the polymer dielectric materials before deposition of the seed layer by Eless copper plating. Mechanical anchoring is the origin of the strong adhesion between copper and polymer layers in this process. However, the large roughness at the dielectric-copper interface induces additional electrical insertion loss,

especially at higher frequencies because of the skin effect [74]. Moreover, large surface roughness results in large amount of side-etching during the seed layer removal process[75]. As indicated in Figure 3.8, copper patterns get narrower because of the isotropic nature of wet etching during the seed removal processes. The extent of narrowing depends on the etch depth, which is the sum of seed layer thickness and roughness factor Rz, which is the average distance between the highest peak and the lowest valley in each sampling length on the dielectric surface. Narrowing of the conductive wiring can be compensated by designing wider conductor line structures. For example, if the etching depth is 3 μm and the target structures have 10 μm line width and 10 μm spacing, the designed structures should be 13 μm line width with 7 μm spacing before etching. The issue with this approach is that room for the compensation decreases and eventually diminishes as the wiring pitch shrinks. To achieve 2 μm conductor wiring with 2 μm space structures (4 μm pitch wiring), the amount of compensation (= etching depth) should be much less than 2 μm. Since the typical roughness factor Rz of the current film dielectric materials is more than 3 μm, fabrication of conductor lines below 5 μm pitch is highly challenging. Reduction in the seed layer thickness can also contribute to decrease in the etching depth, however, a minimum thickness is required to provide sufficient coverage of the seed layer inside the micro-vias for high electrical yield. To achieve excellent seed coverage in micro-vias, deposition of seed layers as thick as 0.3 μm is typically required. Therefore, the target Rz of the dielectric material should be significantly below 0.7 μm to accommodate 2 μm lines and 2 μm spaces (4 μm pitch) conductive wiring structures, so that the required compensation of line structure is well below 1.0 μm.

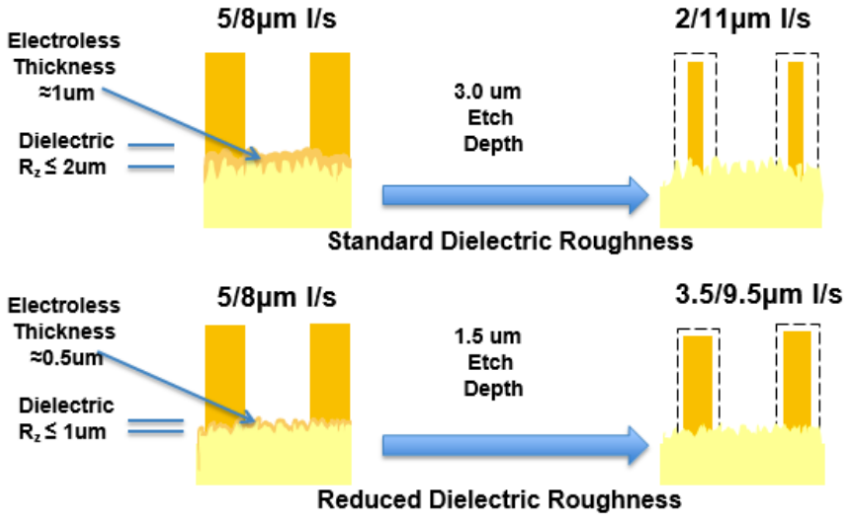

Figure 3.8 Schematic showing the side etching of Cu structures after seed layer removal [75]

Although surface roughness can be reduced by shorter desemar treatment time, it results in weaker bonding between the dielectric and copper layers [47]. Weak adhesion may cause delamination at the interface under thermal excursions during substrate fabrication and assembly processes, or during thermal cycle testing. Therefore, a new approach to achieve stronger adhesion with lower copper to polymer interfacial roughness is required. Several groups reported enhanced adhesion without roughening using chemical bonding or adhesion promotors [49-54]. However, these alternative processes can cause issues at the micro-via connections or can reduce adhesion after highly accelerated stress testing (HAST) under high temperature and moisture.

3.3 New Dry Film Polymer Dielectric Material for Next Generation RDL

This section describes new dry film dielectric materials based on the material design to achieve the desired properties.

3.3.1 Thermoplastic vs. Thermoset Polymer Materials

Dry film dielectric materials need to flow very well during the lamination process for high degree of planarity (DoP), while they need to have high thermal, mechanical and chemical resistance and strong bonding to base materials after the lamination process. Polymer materials are ideally suited for thin film dielectric application due to their compliance, processability and adhesivity. There are two categories of polymer materials; thermoplastic and thermoset. Most of the low temperature thermoplastic polymer materials have poor resistance to high temperatures and cannot survive a solder reflow process at 260 °C. There are high temperature thermoplastic materials such as super engineering plastics that have quite high temperature resistance with excellent properties [34]. However, such materials require high temperature lamination processes over 250 °C to achieve proper flow and bonding for the formation of each RDL layer due to their high softening temperature, which can compromise the dimensional stability of RDL layers. On the other hand, thermoset polymer materials can be processed at low temperatures below 200 °C and have high glass transition temperatures once cured (typical Tg about 150-200 °C). Even though Tg of thermoset materials are generally below the solder reflow temperature at 260 °C, they have excellent dimensional stability due to the cross-linked polymer network. Hence, thermoset polymer materials have a huge advantage for

high density RDL, and the material design in this study will be based on the thermoset polymer system.

Table 3.3 summarizes the electrical properties of the major thermoset polymer materials [76]. As discussed above, low Dk and Df is required for high speed digital signal transmission. From Table 3.3, epoxy, silicone and polyurethane have lower Dk and Df values among the thermoset polymer materials. Among these three, polyurethane has a low relative temperature index (RTI). RTI represents the maximum temperature for a material at which its critical properties will not be unacceptably compromised by chemical or thermal degradation. RTI of polyurethane is much lower than other materials, mainly due to the lower degree of crosslinking. Therefore, epoxy or silicone materials have advantages since the materials should be resistant to the solder reflow temperature of 260 °C. In addition to the thermal stability, adhesion of the polymer materials to metals is one of the important characteristics for RDL wiring. While epoxy based polymer systems have strong adhesion, silicone has quite weak bonding strength to metals. From these analyses, this research focuses on the design of thin film material using an epoxy base polymer. One of the challenges in the conventional epoxy materials is their high dielectric loss of 0.02. As discussed in the previous section, Df of the material needs to be less than 0.01, therefore additional strategy to reduce the Df of epoxy-base polymer dielectric needs to be implemented. The next subsection introduces a new concept to reduce Df of the epoxy-based dielectric material.

Table 3.3 Electrical properties of thermoset polymer materials

Polymer	Relative temp. index (°C)	Dk (@100Hz)	Df (@100Hz)	Dielectric strength (kV/mm)
Epoxy	175	3.2	0.02	19.7
Melamine	150	8.4	0.05	11.0
Phenolic	150	7.0	0.06	15.7
Polyester	130	6.0	0.04	16.5
Silicone	205	5.0	0.01	17.7
Polyurethane	50	3.3	0.03	22.0

3.3.2 Concept of the New Dielectric Material

To address the issue of the current epoxy-based dielectric materials, a new material system with ring-opened norbornene type polymers (NPs) is proposed in this study to achieve the desired properties. NPs are synthesized through the ring-opening olefin metathesis (ROMP) and hydrogenation [77], and Figure 3.9 shows the synthetic routes of NPs. NPs have superior properties for electronic packaging applications, such as low moisture uptake, thermal and chemical stability, low dielectric constant (Dk), and dissipation factor (Df). These excellent properties are originated from their polymer backbone structure, which is composed only of carbon and hydrogen atoms, and rigid and amorphous nature of the polymers.

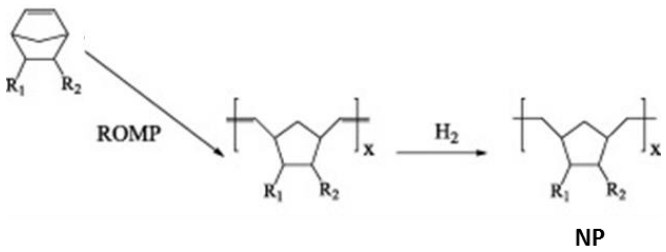

Figure 3.9 Synthetic route of ring-opened norbornene type polymer (NP) [78]

Although NPs have a variety of attractive properties, the use of pristine NPs for RDL dielectric materials is challenging since NPs are thermoplastic polymers. Therefore, this study proposes the new dielectric material (Material A), which includes a copolymer of epoxy and NP units, and silica filler particles. By incorporation of NP units into epoxy moiety, Material A can be processed as a thermoset material and exhibits excellent thermal, mechanical and chemical resistance after curing process. Due to the superior electrical properties of NP, Material A has lower dielectric constant and much lower dielectric loss compared to the conventional epoxy based build-up material. Lower moisture uptake of Material A is another advantage because absorbed water degrades the chemical stability of the polymer and its electrical performance. Material A has lower CTE and higher Young's modulus compared to the conventional materials because it has a larger amount of silica filler inside. Importantly, Material A is compatible with the conventional electroless (Eless) Cu plating process for seed layer formation because it has epoxy backbone in the polymer unit. Table 3.4 summarizes the properties of Material A compared to the conventional epoxy-based dielectric material.

Table 3.4 Properties of conventional epoxy-based polymer dielectric and Material A

Properties	Conventional	Material A
Tg (°C)	153	162
CTE (ppm)	39	25
Young's modulus (Gpa)	5.0	7.0
Dk (at 1GHz)	3.2	3.0
Df (at 1GHz)	0.018	0.006
Water absorption with 100°C, 1h (%)	1.0	0.2

3.3.3 Electrical Performance of the New Material

The electrical performance of the Material A and the conventional material was assessed using electrical signal transmission in a micro-strip line test structure. Figure 3.10 shows the micro-strip line structure used in this test, which was designed to have 50 ohm impedance.

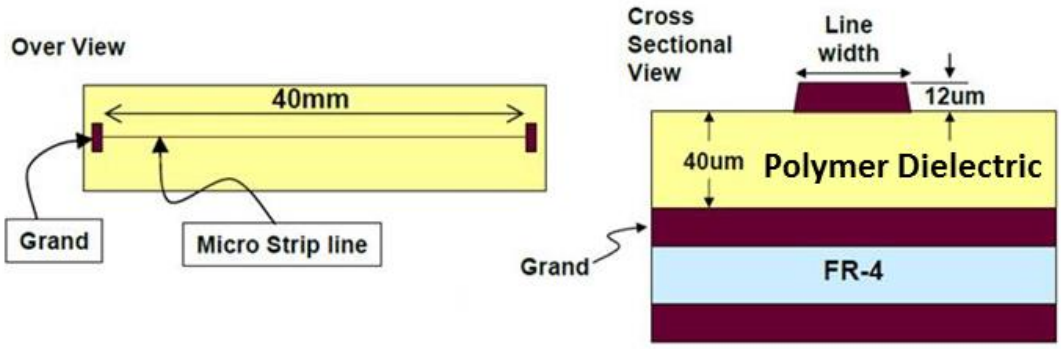

Figure 3.10 Configuration of the micro-strip line for signal transmission test

S parameter measurements were conducted up to 40 GHz using a vector network analyzer and the measured insertion loss (S_{12}) is plotted in Figure 3.11. It is obvious that the signal loss of the micro-strip line with Material A was much lower than that with the conventional dielectric material. The measured insertion loss of transmission line in Material A was almost the half of that the loss of one in the conventional material at 40 GHz. It should be noted that the dielectric loss of Material A is 1/3 of the conventional material, but observed signal loss was not 1/3, because there is a contribution of conductor loss that is common to both materials. The low transmission loss is highly beneficial for high speed digital signal transmission.

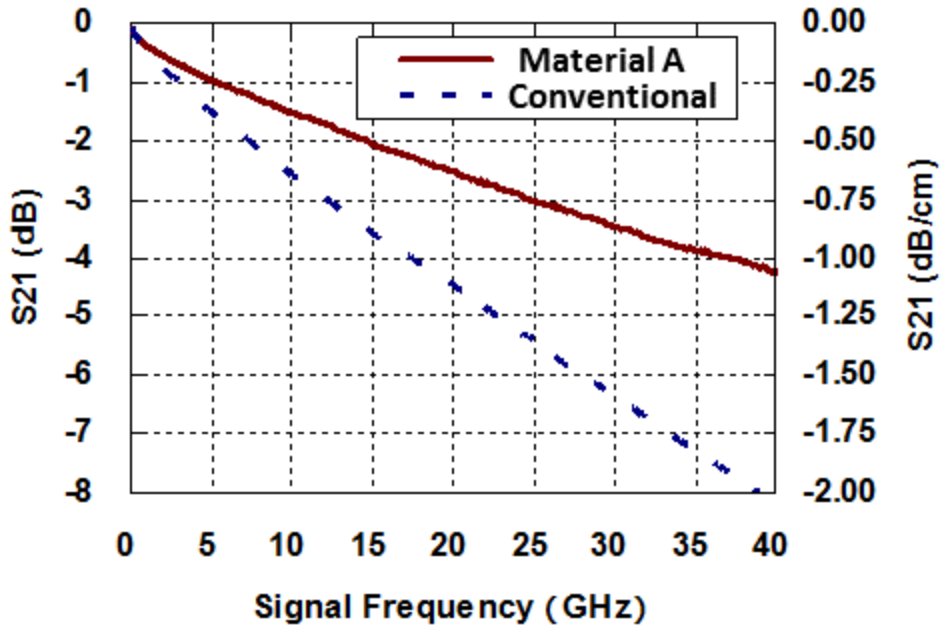

Figure 3.11 Insertion loss (S21) of the high frequency signals of the micro-strip line with different dielectric materials

3.3.4 Adhesion Property of the New Material

Adhesion of the conventional dielectric materials to metal layer is based on the mechanical anchoring effect of the micron-scale surface roughness made by desmear process. Desmear processes include strong oxidation by permanganate and sodium hydroxide, which attack the epoxy polymer matrix to make the surface rough. Since polymer matrix of Material A has NP unit, which is highly resistant against oxidation by permanganate [50], lower surface roughness of Material A after desmear processes is expected. To see the effect of the incorporation of NP moiety into epoxy unit, roughness of the Material A and the conventional material was measured. First, 15 μm thick dry

film dielectrics, Material A and the conventional material, were laminated onto 300 μm thick FR-4 core materials. Then desmear processes, including 15 minutes of swelling, 15 minutes of permanganate oxidation and 4 minutes of neutralization, were applied to the samples. Roughness of the samples after desmear treatment was measured by Olympus LEXT 3D confocal microscope. Profiles of the sample surface and the roughness factor Rz are shown in Figure 3.12. As can be seen, roughness of Material A was below 0.5 μm and much lower than that of the conventional material. This indicates much less oxidation damage in Material A due to the presence of chemically inert NP unit in the polymer backbone, resulting in lower surface roughness after the desmear treatment.

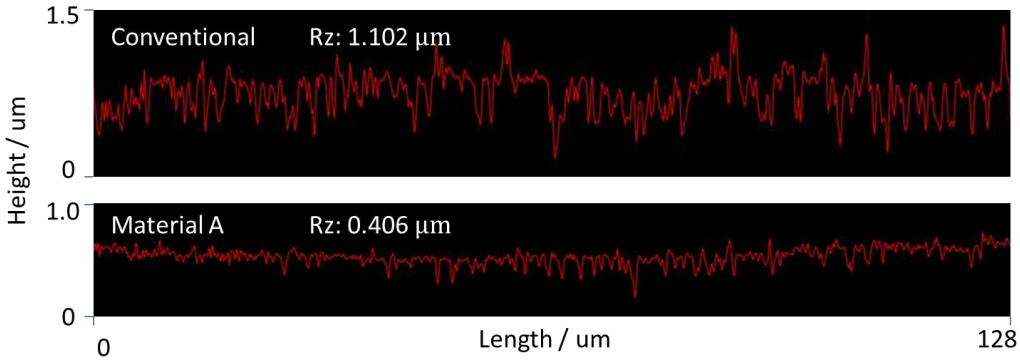

Figure 3.12 Roughness profile of the conventional material (top) and Material A (bottom) after desmear processes

Surface morphology of the dielectric materials after desmear process was observed by scanning electron microscope (SEM) and the pictures are shown in Figure 3.13. Much smoother morphology is confirmed on the surface of Material A.

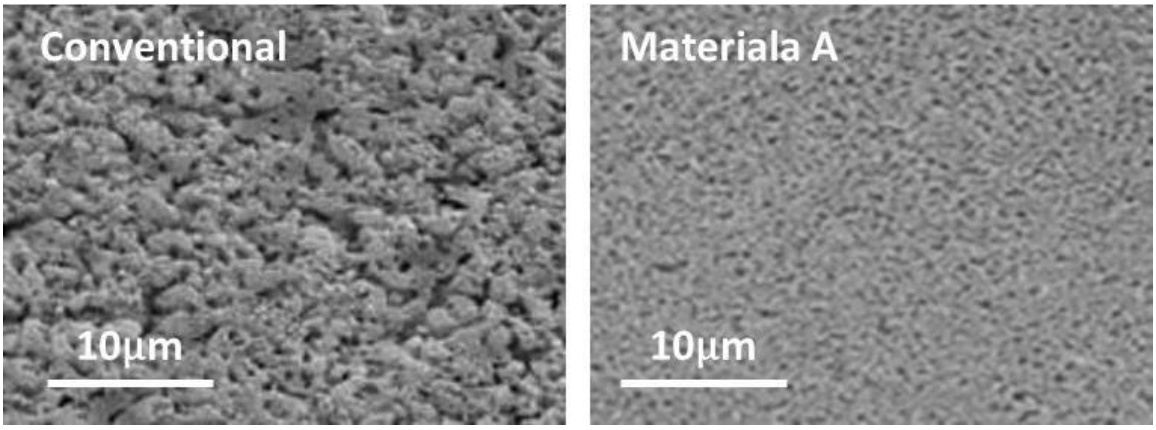

Figure 3.13 SEM image of the surface of the conventional material (left) and Material A (right) after desmear treatment

As a result of much lower surface roughness of the material, interface roughness between the Material A and copper layer was reduced and the cross sectional view of the interface is shown in Figure 3.14.

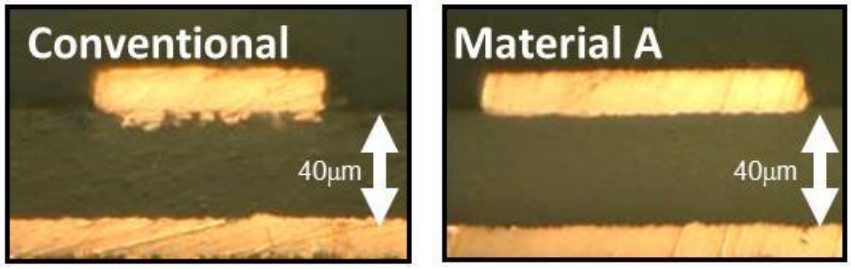

Figure 3.14 Interface of the copper layer and conventional epoxy-based conventional material (left) and Material A (right)

Such smooth interface between the copper layer and dielectric layer is highly beneficial for fine line formation with less side etching, however, it could lead to weaker bonding strength of the plated Cu layer to the polymer surface due to the lack of

mechanical anchoring. To check the adhesion of the polymers to copper layers, peel strength of copper on the conventional material and Material A was measured. Sample preparation for peel testing schematics were: 1. lamination of 15 μm thick Material A or the conventional material on FR-4 core, 2. Desmear and Eless Cu plating (0.2 μm thick seed), 3. Electrolytic Cu plating with 30 μm thick copper, 4. Post-curing at 190 °C for 1 hour. To see the stability of the bonding under high temperature and humidity, highly accelerated stress test (HAST) in a pressure cooker chamber at 85% RH and 130 °C for 100 hours was applied to the samples to see the stability of the adhesion of these materials. Figure 3.15 shows a representative graph of peel strength measurement of 1 cm stripe of the copper layer. The peel strengths were measured as average values of four measurements for each sample. Table 3.5 summarizes the peel strengths between dielectric materials to copper layers before and after HAST treatment.

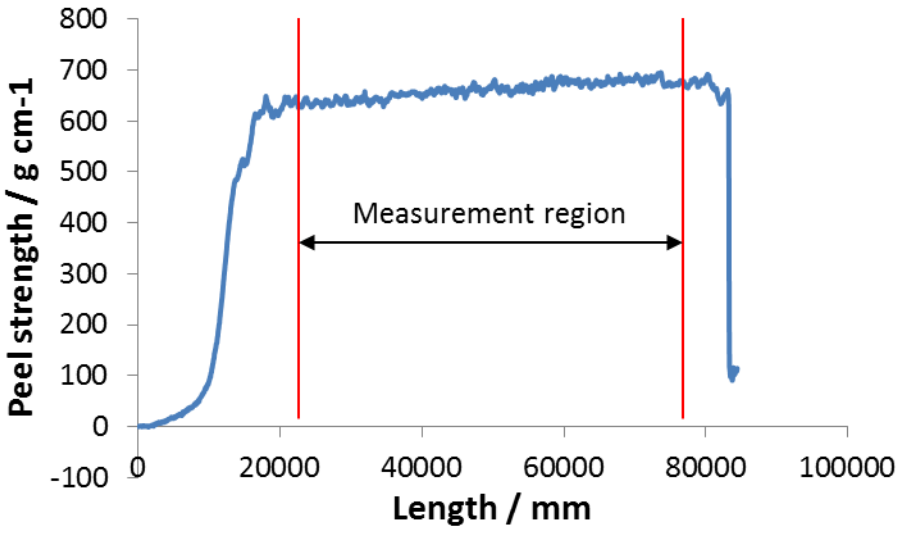

Figure 3.15 Representative peel force measurement of 1 cm Cu strip on Material A before HAST

Table 3.5 Peel strength (N cm^{-1}) of the conventional material and Material A before and after HAST treatment

Peel strength N/cm	Conventional	Material A
Before HAST	0.57	0.66
After HAST	0.57	0.64

Despite much lower surface roughness and chemical inertness, Material A showed strong and highly stable adhesion as well as the conventional material does, before and after HAST testing. To investigate the mechanism of the strong bonding with less roughness between the Material A and copper, micro-scale cross-sectional analysis was conducted with scanning transmission electron microscopy (STEM) to see the detail surface morphology. STEM provides the contrast of the different components at the nanometer level, therefore it is useful for the interface analysis. The interface of the typical epoxy-based material and copper layer was reported to have a sharp contrast as illustrated in Figure 3.16 [53].

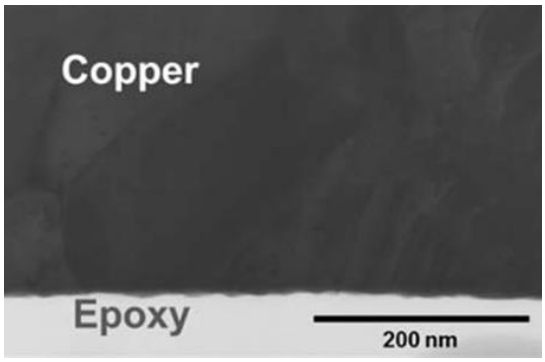

Figure 3.16 Cross sectional STEM image of electroless plated copper on conventional epoxy-based dielectric after desmear process. Image from reference [53]

In contrast, the interface of Material A and electroless copper showed 300-400 nm thick of Cu and polymer mixture layer that forms nano-scaled roughness in between the polymer and copper layers as shown in Figure 3.17. This nano-scale anchoring can strongly bond these layers with much less surface roughness. Such the structure can be caused by the local oxidation of the epoxy moiety in Material A, while imposed minimal damage in the NP moiety.

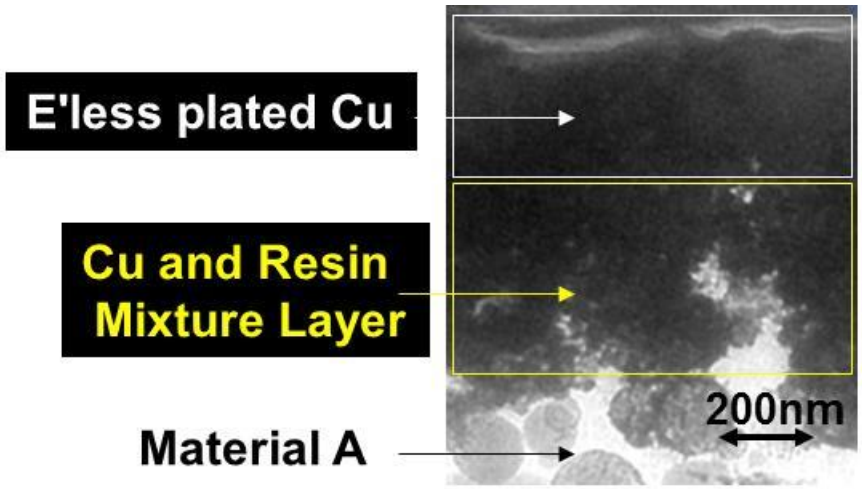

Figure 3.17 STEM image of the cross-section of the interface between electroless plated Cu and Material A

As a result of highly smooth surface, Material A enabled much finer wiring formation by traditional SAP with Eless seed Cu layer. Photolithography with 7 μm thick dry film photo resist was used to pattern the fine pitch wiring structures. Figure 3.18 shows the 4 μm pitch and 3 μm height Cu wiring structures. The structure was designed as 2.5 μm line and 1.5 μm space for compensation of the side etching. After the etching

of 0.3 μm thick Cu seed layer, wiring structure with 1.5 μm line and 2.5 μm space was successfully fabricated. The amount of side etching was 1.0 μm, which is close to the sum of Rz (0.5 μm) and the seed layer thickness (0.3 μm). Therefore, much smooth interface of Material A is confirmed to be highly beneficial in fine line formation with SAP by reducing the side etching of conductor lines during the seed etching step.

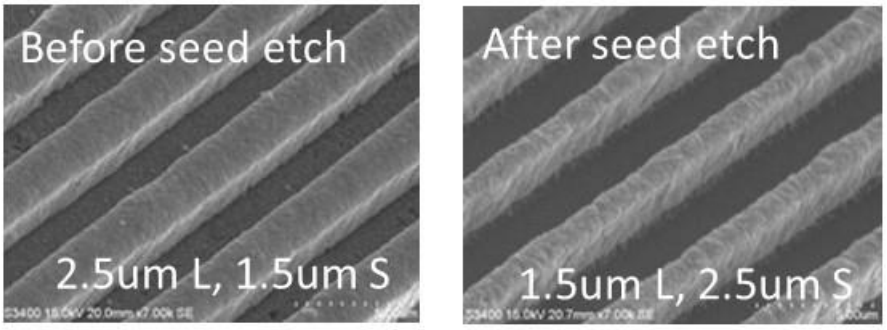

Figure 3.18 SEM image of the 4 μm pitch line and space Cu line structures before (left) and after (right) of seed layer etching. (seed Cu thickness: 0.3 μm)

3.3.5 Ultra-thin Dry film Material

As discussed in the section 3.2.1, thickness of the dielectric needs to be 3-6 μm to accommodate 50 ohm impedance matching to 2 μm ultra-fine copper wirings. To achieve the target, a 5 μm thick dry film of Material A was prepared and the flowability of the material for multi-layer RDL was tested. As discussed earlier, high planarity of the surface after the lamination is one of the advantages of the dry film dielectric material for multi-layer RDL formation. However, as the thickness of the dry film materials decreases, material flow generally becomes smaller, which can cause insufficient flow and undulation of the surface where the wiring structures exist underneath the materials.

In this subsection, surface planarity after the lamination of 5 μm thick dry films of Material A was tested. First, wiring structures with 4.5 μm height were formed on glass core by SAP process. Then 5 μm thick Material A was laminated by vacuum lamination at 100 °C for 2 minutes and hot presses at 110 °C, 1 MPa for 5 minutes. Finally, the dielectric was cured in the oven in air at 180 °C for 30 minutes. Cross section view of the sample is shown in Figure 3.19. Polymer on top of the Cu wirings was about 2.5 μm thick, that means the total thickness of the polymer increased to 7 μm after lamination due to the volume of Cu wirings. As observed, polymer surface was quite flat without undulation on the Cu wiring structures. This indicates the high flow of the polymer during the lamination process even very thin dry film platform.

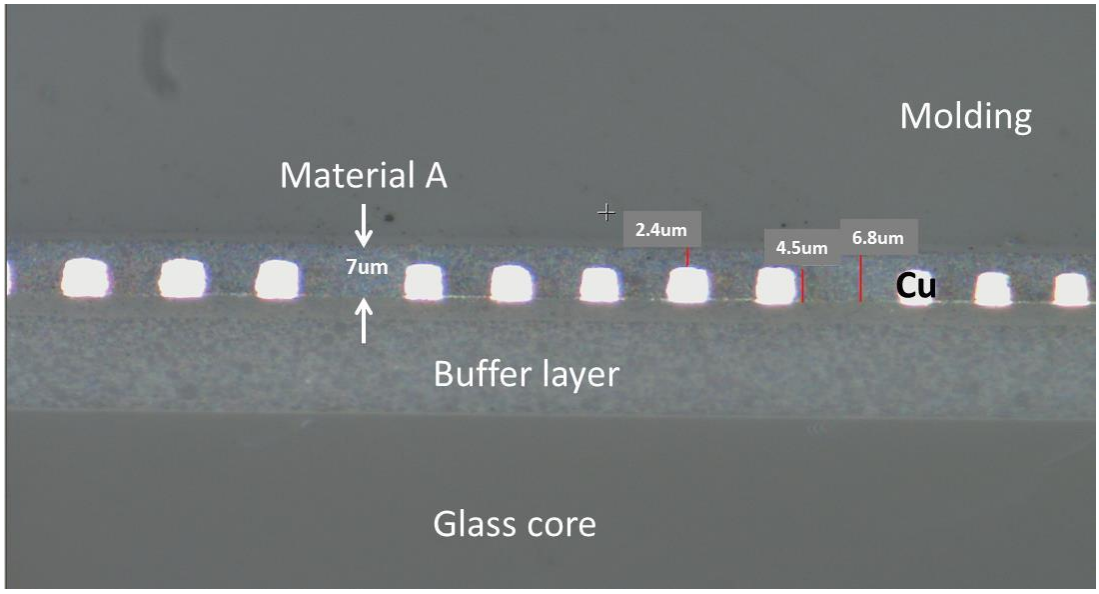

Figure 3.19 Cross section view of the 5 μm dry film Material A on 4.5 μm thick Cu wiring structures

3.3.6 Multi-layer RDL Demonstration and Mechanical Reliability of the New Material

Mechanical reliability of the RDL stack-up structure using Material A was tested. The multi-layer RDL structure was fabricated on 300 μm thick glass core. First, 10 μm thick Material A was laminated on the glass core by vacuum lamination at 100 °C for 120 seconds, then cured at 180 °C for 30 minutes in air. After the lamination, the first metal layer was patterned by SAP process, followed by the lamination of another layer of 10 μm thick Material A. Subsequently, micro-vias with 10 μm diameter were formed in the dielectric layer by excimer laser ablation to interconnect the top and bottom metal layers. Finally, the top metal layer was patterned by SAP process to complete the sample fabrication. The multi-layer RDL was designed as daisy-chain structure for testing the electrical resistance as illustrated in Figure 3.20. There were two types of design with different micro-via pitches at 20 or 40 μm.

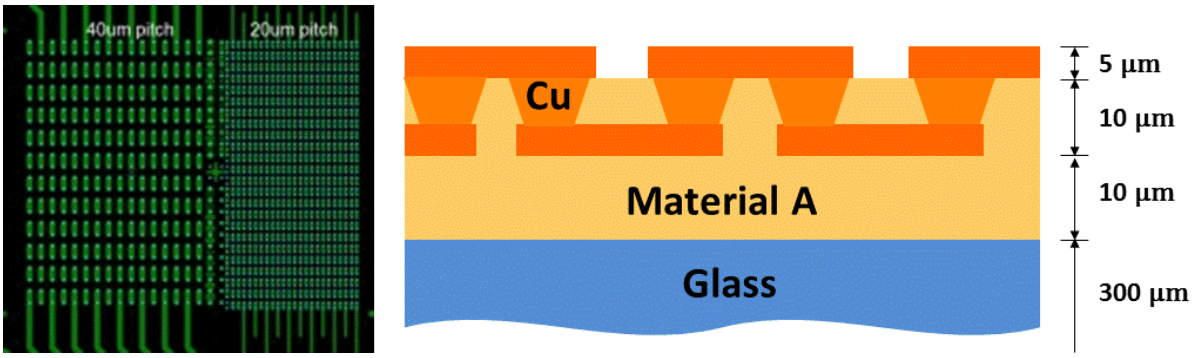

Figure 3.20 Top view (left) and cross section view (right) of the designed daisy-chain structure

After the fabrication, the samples were applied to the MSL3 pre-conditioning, which includes the baking at 125 °C for 6 hours, humidity soaking at 60 °C, 60%RH for 40 hours, and 5 times of solder reflow process at 260 °C. Finally, temperature cycling stress

testing was conducted between -55°C and 125 °C with 15 minutes of dwell time [41]. The electrical resistance of the daisy-chain structures were measured after the fabrication, pre-conditioning, 200, 500, 1000, 2000, 3000, and 4300 cycles. There was no failure observed (failure criteria: 20% increase in resistance) up to 4300 cycles with the coupons of both designs. A typical requirement of the multi-layer RDL reliability is 1000 cycles without failure. Therefore, this result demonstrates the quite high reliability of the multi-layer RDL structure using Material A due to its low CTE and resulting low stress.

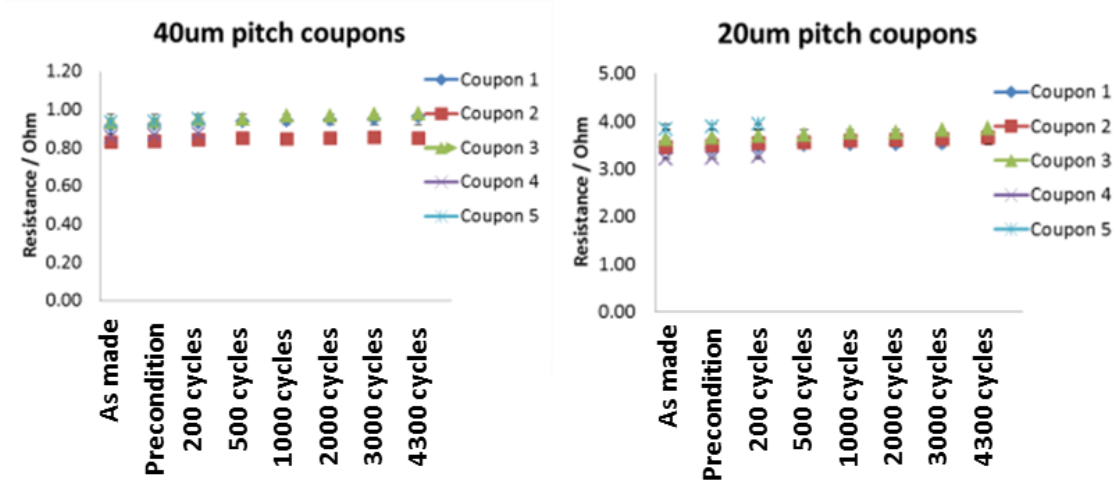

Figure 3.21 Electrical resistance of the daisy-chain coupons of 40 µm pitch structure (left) and 20 µm pitch structure (right)

This chapter reported the material design to clarify the need for RDL dielectric materials, the demonstration of a new material, and characterization of the material performances. Material A satisfies the required properties and enables 2 µm wiring structure by SAP due to nanometer scale roughening. However, there is a still limitation in scaling of fine line formation by SAP, despite the progress made by the new material.

The limitation includes high line resistance of the narrow line due to side etching, and challenge in photolithography patterning. Although side etching can be compensated for small amount by designing the wiring structure fatter at the beginning, it requires narrower photo resist line structure instead. As the line pitch decreases, aspect ratio of the photo resist line gets extremely large (Figure 3.22) and photolithography processing becomes more challenging due to the collapse of very narrow photo resist lines. For example, 1 μm photo resist line structures need to be fabricated for compensating 1 μm of side etching, in order to achieve 2 μm line and space copper wirings. Current dry film photo resist thickness is 5-7 μm, therefore line structure with aspect ratio larger than 5, which is highly challenging, is required.

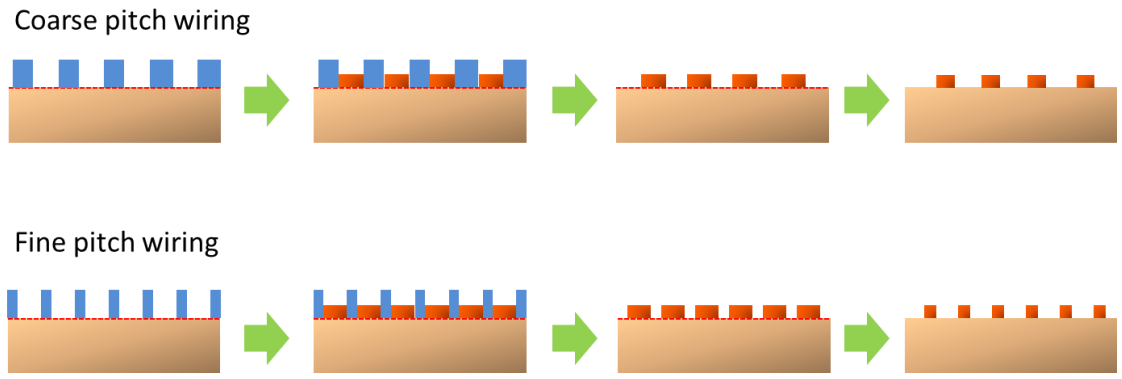

Figure 3.22 Decreasing line width of photo resist structure as reduction in line pitch

3.4 Chapter 3 Summary

Design of a material to achieve the required electrical, thermal and adhesive properties was performed in this chapter to clarify the target for RDL dielectric materials. Electrical design was performed based on 50 ohm impedance calculations and high speed

signal transmission loss. As a result, thickness of a dielectric material is required to be 3-6 μm and dielectric loss needs to be below 0.010. Thermo-mechanical design based on the finite element modeling (FEM) revealed that the dielectric CTE below 32 ppm/°C is desirable for high reliability of RDL structures. Assessment of side etching of copper line during the seed etching step requires the surface roughness Rz well below 0.7 μm.

After the material design, epoxy-NP copolymer based new dielectric materials for meeting the required properties was introduced. The analysis of electrical, thermo-mechanical and adhesion properties of Material A showed the superiority of Material A compared to the conventional epoxy-based dielectric materials. Excellent surface planarity after the lamination of a 5 μm thick dry film of Material A was confirmed without undulation on the copper structures underneath. In depth analysis of the bonding mechanisms of Material A revealed that nano-scale anchoring contributed strong adhesion of the polymer to copper layer while reducing the interface roughness. As a result, copper wiring structure with 1.5 μm line and 2.5 μm space was successfully fabricated.

CHAPTER 4. ULTRA-SMALL MICRO-VIA AND WIRING PROCESSES IN ULTRA-THIN POLYMER DIELECTRICS

This chapter describes the research into ultra-small micro-via and conductor wiring processes to form multilayer RDL structures at 20-40 µm pitch in ultra-thin dry film polymer dielectrics. The polymer materials were selected based on the design from first principles discussed in detail in Chapter 3. Traditional SAP methods to form RDL wiring have been limited in scaling to 5 µm wiring [79-81], and face several challenges in scaling below 5 µm. The process limits are the side etching of the copper lines during seed layer removal and poor adhesion of ultra-fine copper conductor lines on smooth polymer dielectric surfaces. This research explores several new process methods to form trenches and micro-vias in ultra-thin dry film polymer dielectrics, and also demonstrates a new integration method to address the scaling challenge of semi-additive processes (SAP) by eliminating side etching of the copper lines. The reduction of the micro-via capture pad size is an important requirement to achieve the target wiring density, and is enabled by improving the positional accuracy of the micro-via formation process and by selection of dimensionally stable core materials. As a core material for this research, glass was selected because of its superior dimensional stability compared to organic laminate composites, low electrical loss and large panel availability [82, 83].

4.1 Mask Projection Trench and Micro-via Formation Processes in Ultra-Thin Polymer Dielectrics

This section presents the research on processes to form 2-5 µm wide trenches and 5-10 µm diameter micro-vias in 5-10 µm thin dry film polymer materials using two new high throughput, highly parallel structuring processes by mask projection of circuit images. The process flow for forming multilayer RDL structures using a new "embedded copper" process is shown in Figure 4.1. Micro-vias are required for vertical layer to layer electrical interconnections for all types of copper conductor formation processes. The trench structures are part of the new embedded copper RDL process that emulates a dual-damascene process used in silicon wafer BEOL RDL, but uses ultra-thin polymer dielectric materials in place of the silicon dioxide thin films on silicon interposers. This embedded copper process eliminates the need to wet etch the copper or Ti-Cu seed layers, that are the main limiting factor in dimensional scaling of current SAP processes.

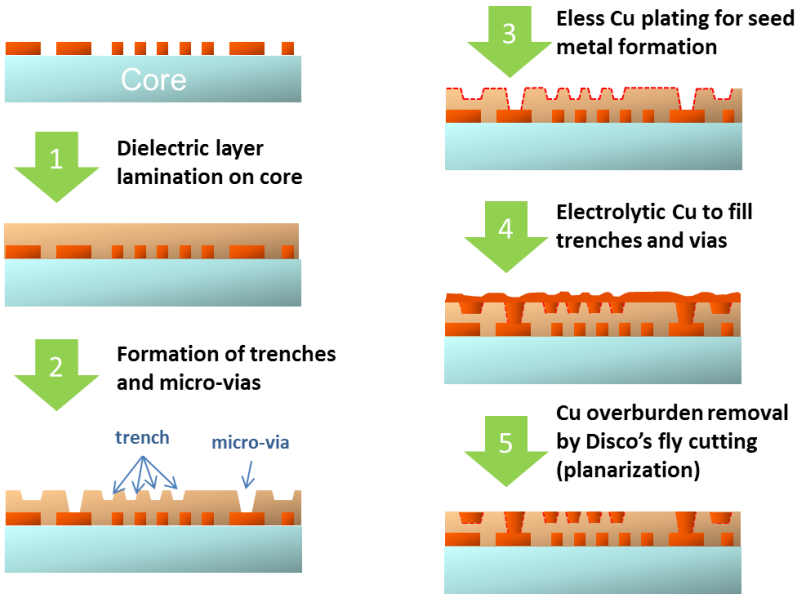

Figure 4.1 Process schematic of the new embedded copper process

The trenches and micro-vias for high density RDL have four critical requirements; (a) trench width and spacing smaller than 5 μm, and micro-via diameter less than 10 μm, (b) high positional accuracy of 1-2 μm, (c) high process speed, and (d) high reliability of the finished RDL structures. However, none of the current processing methods for polymer dielectrics satisfy all of these requirements. This dissertation research explores two processes with the potential to meet all the requirements defined above. These two highly parallel processes use mask projection to define the trench and via locations, resulting in higher positional accuracy (1 μm), at much higher process speeds compared to serial laser processes currently used for dry film polymers. The first approach is atmospheric ozone gas etching, combined with a mask deposition that are patterned by photolithography. The second approach uses nanosecond excimer laser projection ablation through metal mask patterns. The focus of this research was on the fundamental design and analysis of these processes for ultra-small trench and via formation.

4.1.1 Ozone Etching Processes

This subsection presents the first demonstration of trench and micro-via formation in a polymer dielectric layer by an ozone gas etching process [84]. Thin film metal or photo resist etching masks were created on the polymer surface by photolithography, and used to define the trench and micro-via locations for ozone etching. The main advantages of this process are, (a) applicability to a variety of polymer materials due to the high oxidation potential of ozone, (b) accurate via-to-via registration defined by the location of mask openings, and (c) massively parallel generation and high process speed with an atmospheric pressure process.

4.1.1.1 Mechanism of Ozone Etching of Polymers

Ozone gas is a strong oxidant and can decompose a variety of organic substances. It is widely used for disinfection, deodorization, sanitization, bleaching and cleaning processes [85-87]. The mechanism of the polymer decomposition by ozone oxidation has been elucidated for unsaturated polymers, where ozone attacks C=C bonds and creates carbonyl oxides, followed by the separation of the original double bond and the formation of two ketones (Figure 4.2). This auto-oxidation sequence is known as alkene ozonolysis [88]. In the case of saturated polymers, it is believed that the existing C=C bond at the defect site would be the main reaction spot. However, recent research with quantum chemical calculations revealed that the C-H bond in the saturated PMMA polymer is susceptible to oxidation, and polymer decomposition proceeds even without the presence of C=C bonds in the polymer chain. The suggested mechanism begins with the extraction of H atoms from the polymer backbone, followed by hydrotrioxide formation and its auto-oxidation process, leading to fragmentation of the polymer chain (Figure 4.3) [89]. Epoxy polymers are composed of C-H and C-O bonds, therefore the oxidation mechanism can be considered as the primary path for etching by ozone gas.

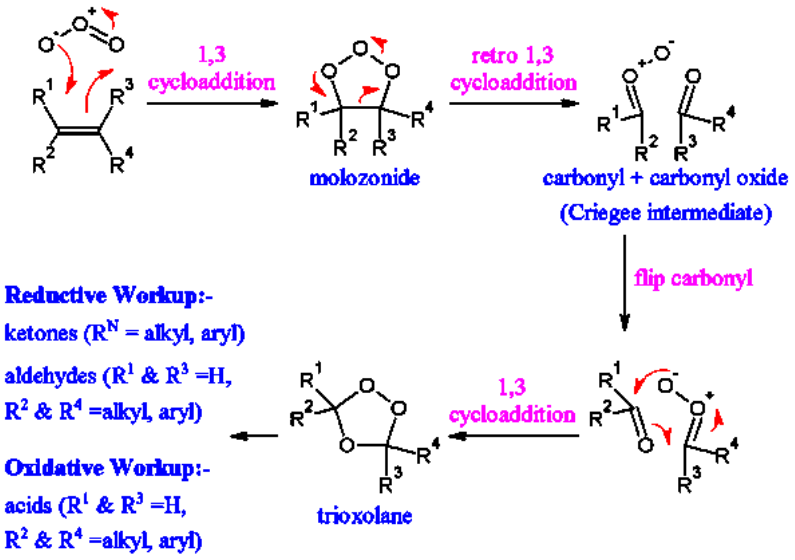

Figure 4.2 Ozonolysis of C=C bonds in unsaturated polymer [90]

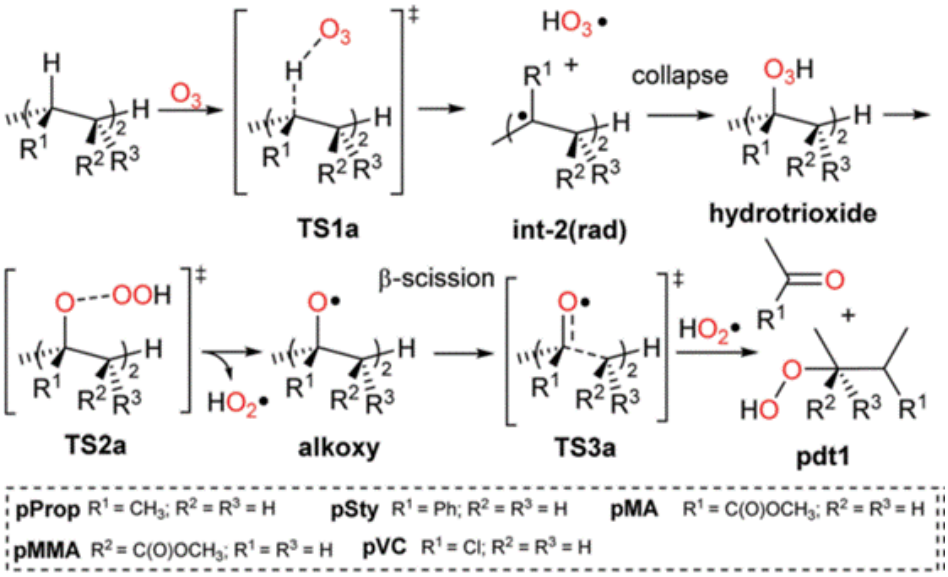

Figure 4.3 Mechanism of the decomposition of saturated PMMA polymer by ozone [89]

In the semiconductor device fabrication process, ozone gas is used for silicon surface cleaning and removal of photo resist (ashing) [91], as well as in deposition of oxide films (TEOS/Oxide) [92]. Compared to these cleaning or surface oxidation processes, much higher reaction speeds are required for etching dielectrics to form trenches and micro-vias. However, ozone gas tends to decompose into oxygen under ambient conditions, therefore achieving a high concentration of ozone gas at atmospheric pressure is very challenging. Ozone gas is generated by three main methods; electrolytic decomposition, UV lamp exposure and silent discharge. This research used a high concentration ozone generator SEMOZON^{TM} AX8410, developed by MKS Instruments, that is based on a silent electrical discharge process. This ozone generator enables production of high concentration (>20%) ozone gas at atmospheric pressure, this is ideally suited for high speed polymer etching.

4.1.1.2 Ozone etching of epoxy polymer

As a first step, the etching rate of a cured epoxy polymer film was determined. The etching rate of the polymer film by an ozone gas process with SEMOZON^{TM} AX8410 was tested at different temperatures under an ozone concentration of 300g/m^3 and the Arrhenius plot is shown in Figure 4.4. The apparent activation energy calculated from this plot was 0.89 eV, which is much higher than 0.24 eV reported for novolac-based photo resists using ozonized water [93]. This higher activation energy is reasonable, considering the polymer dielectric materials are fully-cured whereas photo resist materials are partially cured.

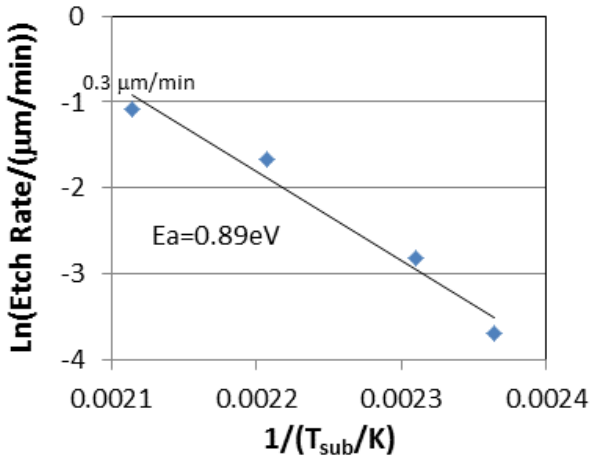

Figure 4.4 Arrhenius plot of ozone etching of epoxy polymer film

To evaluate the efficiency of the ozone etching process for micro-via formation, etching tests were conducted for a build-up polymer ABF GX92, from Ajinomoto, Japan. GX92 is an epoxy-based dry film dielectric used as a standard build-up material. Samples were prepared by laminating 5 µm thick GX92 films on copper clad laminate (CCL) organic core materials. The samples were placed on a heated stage at various temperatures (120; 150; 180; 200 °C) inside an ozone chamber, and then ozone was introduced into the chamber at a concentration of 300 g/Nm^3 for 10 minutes. To assess the impact of the process temperature on the ozone etching mechanism, attenuated total reflection (ATR) Fourier transform-infrared spectroscopy (FTIR) was performed after the ozone process (Figure 4.6). As the process temperature increased, vibration signals originating from the polymer backbone (1230 cm^{-1}: C-O, 1510 cm^{-1}: C-C in aromatic ring, 1740 cm^{-1}: C=O, 2930 cm^{-1}: C-H) weakened. All signals associated with any organic groups were completely diminished after the ozone process at 200 °C and only Si-O bonding signals (810 cm^{-1}, 1050 cm^{-1}: Si-O-Si) from the silica fillers were observed. This indicates

complete oxidation of the epoxy polymer matrix into gaseous substances at 200 °C. Therefore, a process temperature of 200 °C was selected for ozone etching in the following experiments.

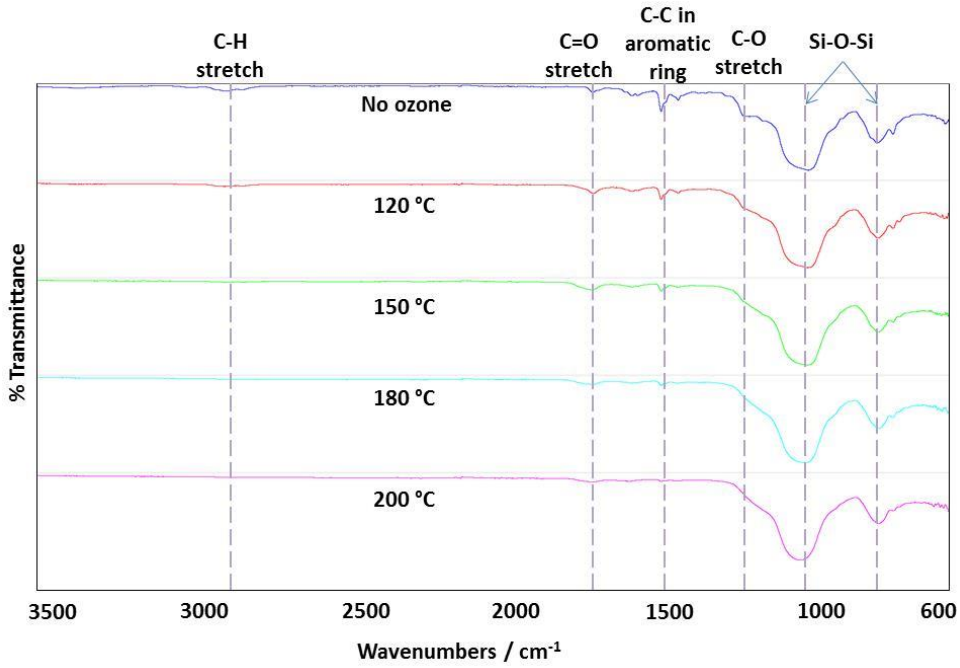

Figure 4.5 ATR FTIR spectra of the GX92 after ozone process at different temperatures

To evaluate the etching speed, various ozone process times were applied to 6 inch × 6 inch square panel samples with the same configuration as in the previous experiments (200 °C temperature, 300g/m^3 ozone concentration). After the ozone process, residual white silica powder was observed on the sample surface (Figure 4.6 left). The white powder comprised of fragmented organic residues and silica filler particles, and was effectively removed by a typical cleaning procedure for the ABF material, namely, chemical desmear cleaning with sodium permanganate and sodium hydroxide. After five

minutes of the desmear cleaning process, the residue was removed and the underlying polymer or copper layers were revealed (Figure 4.6 right).

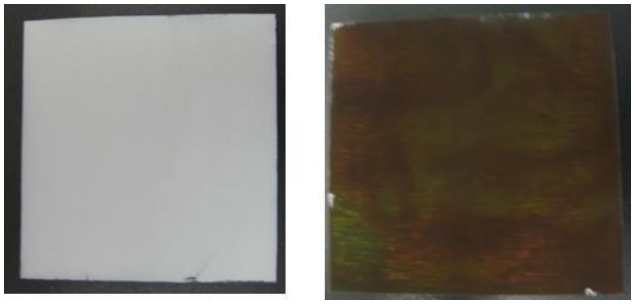

Figure 4.6 Top view of the sample as ozone etched (left) and after desmear cleaning (right)

After the cleaning, the thickness of the dielectric GX92 was measured by surface profilometry and Figure 4.7 summarizes the relative thickness of the dielectric after the ozone etching and desmear cleaning. As the ozone time increased, the dielectric thickness was reduced and complete removal of the dielectric layer was observed after 30 minutes of ozone etching followed by desmear cleaning.

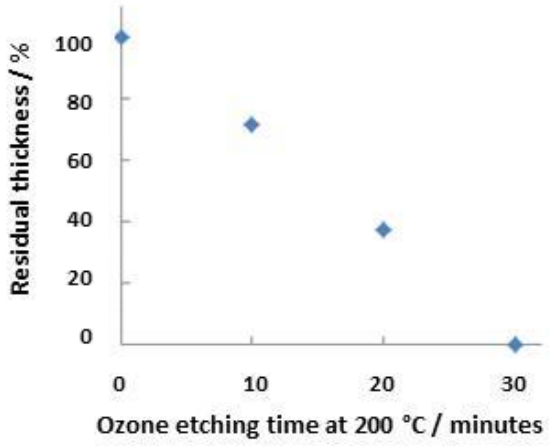

Figure 4.7 Relative thickness of GX92 (5 µm thick originally) after various ozone etching duration times at 200 °C, 300g/m^3

4.1.1.3 Micro-via and Trench Formation by Ozone Process

To form micro-via holes by ozone etching processes, the polymer layer needs to be etched selectively at the micro-via locations. In this study, hard and soft masks were used to define the location and size of the vias. Copper and aluminum thin films deposited by physical vapor deposition (PVD) were used as hard mask materials for their ease of patterning and very low reactivity with ozone compared to other metals [94, 95]. For the soft mask, a negative acting dry film photo resist (PR) was used for its fine patterning capability. Samples were prepared using the process flow described below.

1. Hard mask samples

- 5 μm thick ABF GX92 lamination on Cu clad laminated (CCL) core that comprises 18 μm thick copper foil and 800 μm thick FR-4.
- 0.1 μm thick copper or aluminum layer was formed by sputtering processes
- Lamination of 7 μm thick dry film PR on top of the metal layers
- Photolithography process to pattern 15 μm diameter opening in the PR layer
- Cu or Al chemical flash etching to make a mask pattern in a copper layer to form 15 μm diameter opening in the Cu or Al layer
- Stripping PR off from metal surfaces

2. Soft mask samples

- 5 μm thick ABF GX92 lamination on CCL core
- Lamination of 7 μm thick dry film PR on top of the ABF layer
- Photolithography process to pattern 15 μm diameter opening in the PR layer

After the sample preparation, ozone gas with a concentration of 300 g/Nm^3 was applied at 200 °C for different time durations ranging from 5 minutes to 30 minutes. After the ozone etching, chemical desmear cleaning processes were applied to the samples for five minutes. The hard or soft mask materials (copper/aluminum/PR) were also removed completely during the desmear processes to reveal the polymer surface and micro-vias. After the cleaning, the micro-via profiles were measured with an Olympus LEXT 3D confocal microscope. In the sample with an aluminum mask, uniform reduction of the dielectric thickness was observed regardless of the presence of aluminum on top of polymer layer, which resulted in no micro-via definition in these samples. This indicates that the ozone gas penetrated the aluminum layer without decomposition, contacting the polymer layer underneath and etching it non-selectively. In contrast, successful via formation at the mask opening locations was observed in the samples with copper or PR masks. Figure 4.8 shows the micro-vias formed in a sample with PR mask after 25 minutes of ozone etching and 5 minutes of desmear cleaning processes. Micro-vias with diameters of 17-20 μm and depth of 6 μm were formed in the dielectric layer.

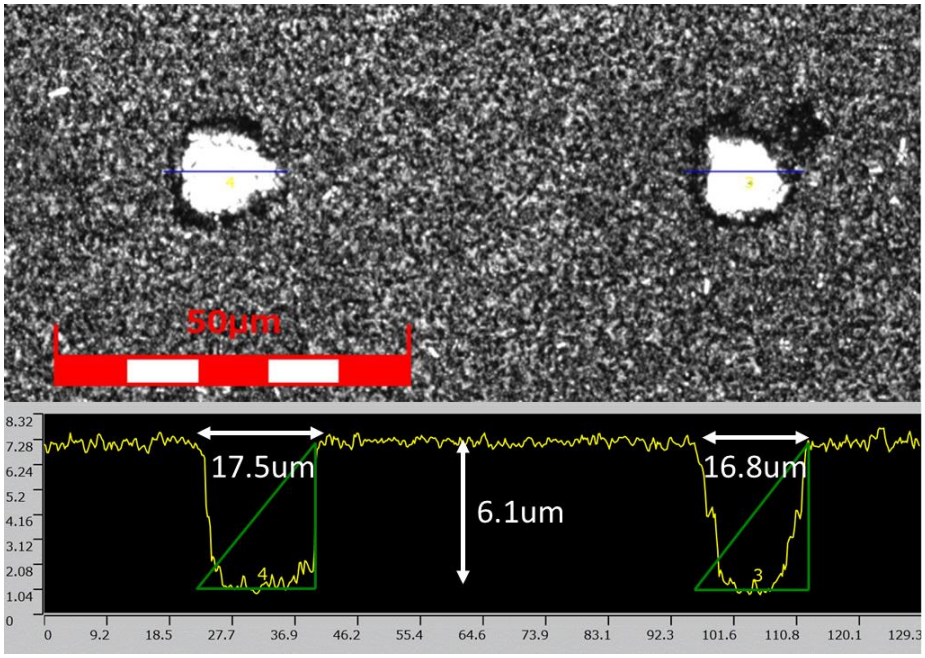

Figure 4.8 Top view and associated profile of etched micro-via array in PR mask sample of 25 minutes of ozone etching at 200 °C, 300g/m^3

Figure 4.9 summarizes the depth of micro-vias and trenches in the samples with different mask materials at different ozone etching times. The values are averaged from the measurement of five micro-vias in each sample. As described above, ozone process applied to the samples with Al mask did not yield any micro-vias due to non-selective etching, therefore no data was plotted for Al mask samples. It was observed that the etching speed of micro-vias and trenches in the sample with PR mask (~0.2 µm/min) was 5 times faster than in the one with the Cu mask (~0.04 µm/min).

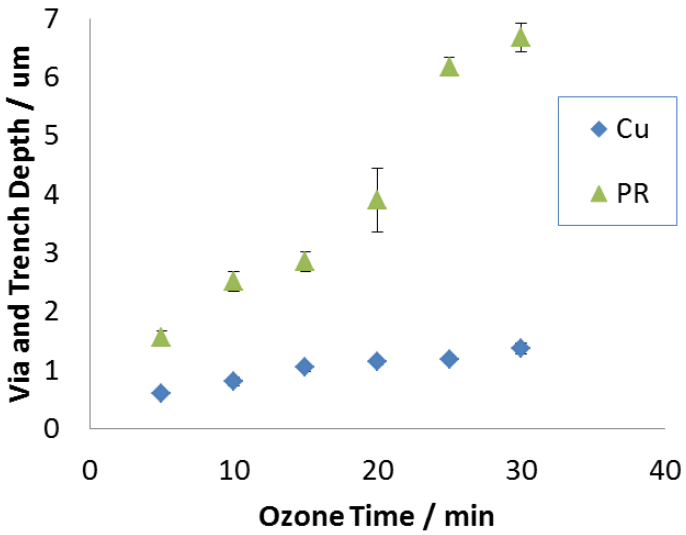

Figure 4.9 Via and trench depth vs. ozone process time at 300 g/Nm^3, 200 °C with different type of masks.

There are two possible causes for the higher etch rate with the PR, (1) the higher surface temperature of the PR mask sample during the ozone process possibly due to the combustion of the organic component in the PR, and (2) locally lower ozone concentration due to the decomposition of ozone gas on the copper mask. To verify these hypotheses, another sample with a Cu hard mask was prepared, but without removing the PR from the top surface (named as PR + Cu mask). Configurations of the samples used in this study are summarized in Figure 4.10.

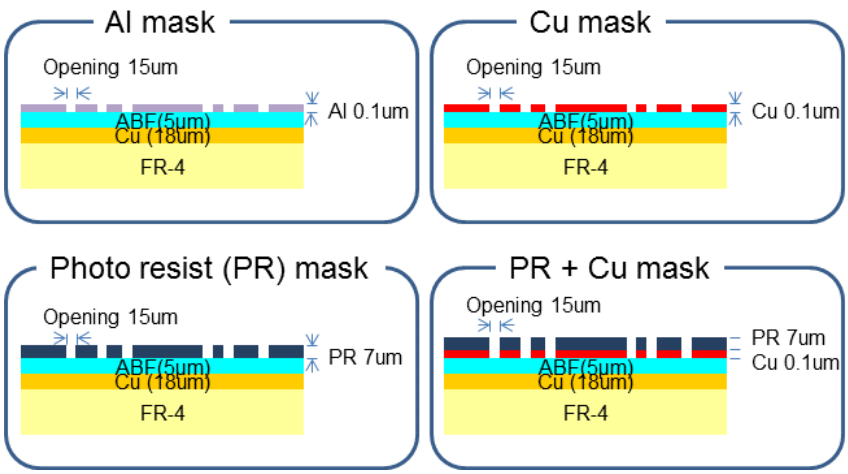

Figure 4.10 Configurations of the samples used in this study

For the initial investigation, the maximum temperature of the sample surfaces during the ozone process were measured using temperature indicator labels by Omega Engineering. No significant differences in the maximum surface temperatures within the smallest scale of the label (5 °C) were observed between the samples with the various mask configurations. Additionally, almost no dimensional change in PR mask openings was observed even after 30 minutes of ozone treatment, which indicates the absence of any reaction in the PR mask material. Average opening sizes at the top of the PR masks and opening heights for 15 measurements were 22.7 µm diameters with 4.6 µm height prior to ozone treatment, and 22.1 µm diameters with 4.3 µm height after the ozone treatment. Figure 4.11 shows the top views and profiles of the PR mask before and after ozone treatment. These results suggest that the different etching speeds may not have originated from the temperature difference of the samples due to the combustion of PR mask (hypothesis 1).

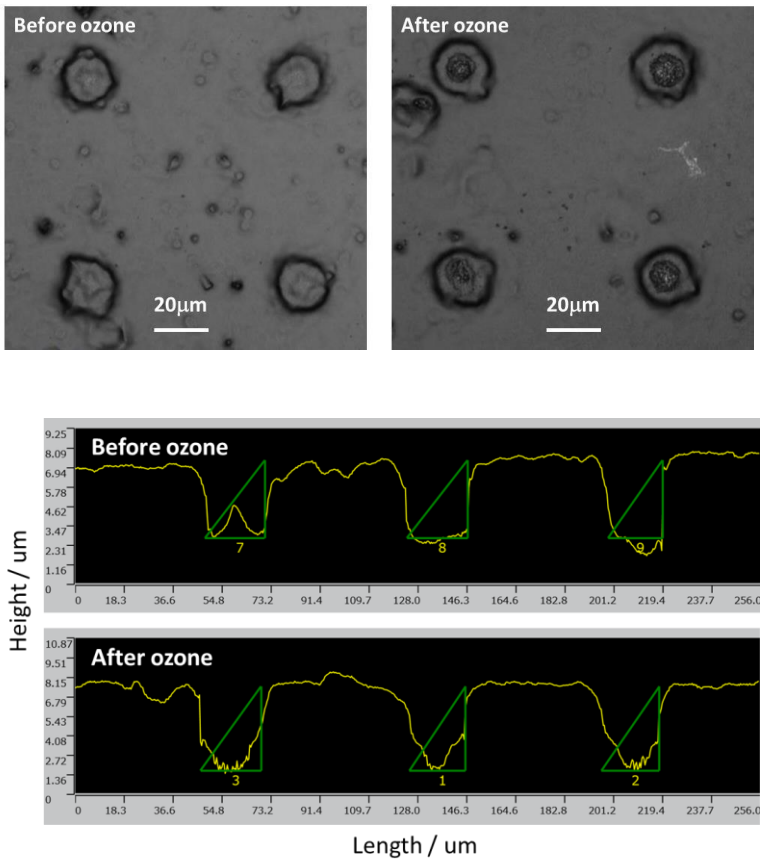

Figure 4.11 Top view (upper) and profiles (lower) of the PR mask openings before and after ozone treatment at 300 g/Nm^3, 200 °C for 30 minutes

For the next experiment, the depth of the micro-vias after ozone etching and desmear cleaning were measured by the confocal microscope, and the results are summarized in Figure 4.12 (the values are the average of five micro-vias in each sample). As illustrated in the graph, the micro-via etching rate in the PR + Cu mask sample was almost the same as the one in the PR mask sample. This result supports hypothesis 2 and indicates that the ozone decomposition was minimized by covering the top side of the copper mask with photo resist and by reducing the amount of exposed copper surface area.

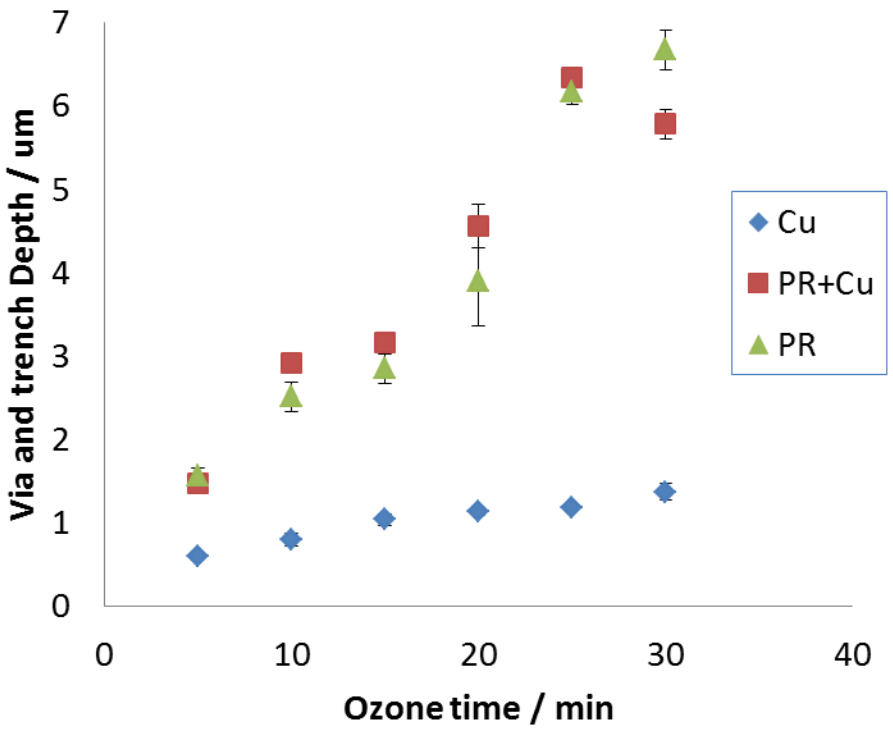

Figure 4.12 Via and trench depth vs. ozone process time at 300 g/Nm^3, 200 °C with different type of masks

After the formation of micro-vias with 20 µm openings of PR mask, 5 µm thick copper was plated on the micro-via structures by electroless (Eless) copper plating and electrolytic copper plating processes. A cross sectional view of the plated micro-via is shown in Figure 4.13. The via opening size was 30 µm diameter with 5 µm depth, which indicates the etching process by ozone was isotropic (20 µm + 5 µm both sides = 30 µm).

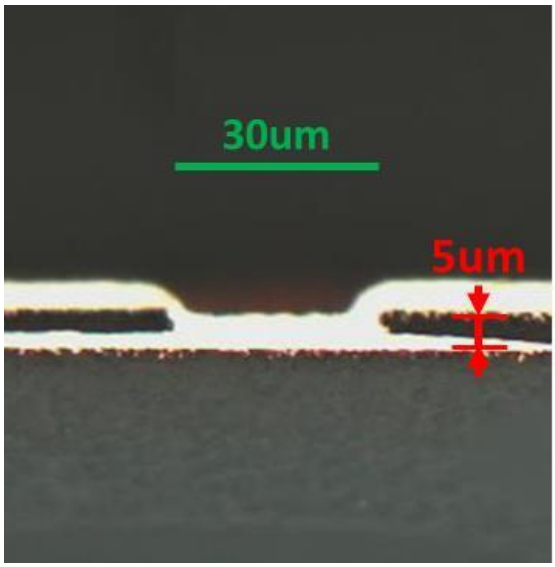

Figure 4.13 Cross section view of the plated micro-via with 20 µm mask opening

This research represents the first demonstration of micro-via formation in thin polymer dielectrics by atmospheric ozone etching processes. From the initial investigation, it has been confirmed that ozone gas is an effective etching agent for the epoxy polymer matrix. Residual silica fillers were easily removed by a conventional wet cleaning process. Ozone processes are environmentally friendlier and potentially higher throughput than conventional plasma etching where fluoride based toxic gases and vacuum processing are required. However, micro-via diameter scaling below 10 µm and trench width scaling below 5 µm faces severe challenges due to the isotropic nature of the ozone etching process.

4.1.2 Excimer Laser Ablation

This subsection describes the demonstration of excimer laser ablation for trench and micro-via formation [96, 97].

4.1.2.1 Mechanism of Excimer Laser Ablation of Polymers

One of the advantages of using an excimer laser is the efficient vertical ablation of polymer materials that enables anisotropic etching of polymer layers. The photon energy of excimer lasers is usually larger than 4 eV, the typical molecular bonding energy observed in polymer materials (C-H, C-C, C-O and other bonds). Additionally, polymer dielectrics have strong absorption of ultra-violet light, in the operating wavelengths of the excimer lasers, which induces efficient photon penetration into the polymer materials. As a result, the absorbed photon of the excimer laser initiates photo-induced sublimation of the polymers from a solid phase to a gas phase [98]. The energy discharged during the transition is converted into the velocity of the decomposed fragments, and this conversion leads to the explosive ejection of the fragments, a process known as ablation [99]. These fragments are ejected out of the polymer layer effectively because the energy of the excited electron goes into an anti-bonding state, generating a repulsive force [99]. The efficient use of ablation leads to the clean etching of the polymer without significant heat damage. Another advantage of the excimer laser is the capability of mask projection processing due to the large beam size [100, 101]. The large beam size enables the formation of ultra-small micro-vias, defined by the mask opening size. Since the locations of micro-vias are defined by the mask, high positional accuracy is guaranteed (below 1 μm), enabling a reduction in capture pad size and accurate layer-to-layer

registration. Furthermore, the capability of mask projection results in high throughput processing using step-and-repeat patterning, and scalability to large panel fabrication [62]. When the laser beams irradiate polymer samples, attenuation of light intensity (I) takes place, as described by Eq. 4-1, where α is absorbance of the material at the wavelength and z is penetration depth, and I_0 is the initial light intensity.

$$I(z) = I_0 \exp(-\alpha z) \qquad \textbf{Equation 4-1}$$

Absorbed energy per unit mass E_m is calculated by Eq. 4-2. (t_p: laser pulse width, ρ: density of mass)

$$E_m(z) = I(z) t_p \alpha / \rho \qquad \textbf{Equation 4-2}$$

E_m should be larger than the threshold energy E_{th}, in order to obtain ablation of the material. The threshold light intensity I_{th} is calculated by I_{th}, = ρ E_{th} /αt_p

The ablation rate per pulse La ~ z can be assessed by Eq. 4-3.

$$L_a = \frac{1}{\alpha} \ln\left(\frac{I}{I_{th}}\right) \qquad \textbf{Equation 4-3}$$

To ensure trench and micro-via formation by laser ablation processing, laser systems with power levels higher than the threshold energy of the material are required. On the other hand, too much fluence has a negative effect, such as too much enlargement of trench and micro-via sizes from the designed values as well as shape distortion.

Excimer lasers are available in different laser wavelengths based on the type of active gases utilized; 157 nm (F2), 193 nm (ArF), 248 nm (KrF), 308 nm (XeCl), 351 nm

(XeF). Ultra-violet (UV) light below 250 nm wavelength is strongly absorbed by glass materials, and therefore, F2, ArF and KrF excimer lasers are useful for glass structuring [102]. However, these lasers cause inherent damage to the optical components made of glass materials, reducing their useful lifetime and increasing the process cost. Additionally, strong attenuation of the laser occurs in air due to absorption by oxygen at ultra-short wavelengths. Therefore, optical paths should be purged with nitrogen or argon, or maintained in vacuum, making the system more complicated and expensive. In this research, a 308 nm XeCl laser was selected because of the radiation inertness in air and due to the minimal damage to the optics while maintaining high processing speeds for polymer materials. Figure 4.14 shows the experimental schematic of an excimer laser ablation system with mask projection. This study used the excimer laser system ELP300 Gen2 from Suss Photonic Systems, Corona CA, equipped with Coherent LPXPro 305 (XeCl) and projection lens with a numerical aperture (NA) of 0.1.

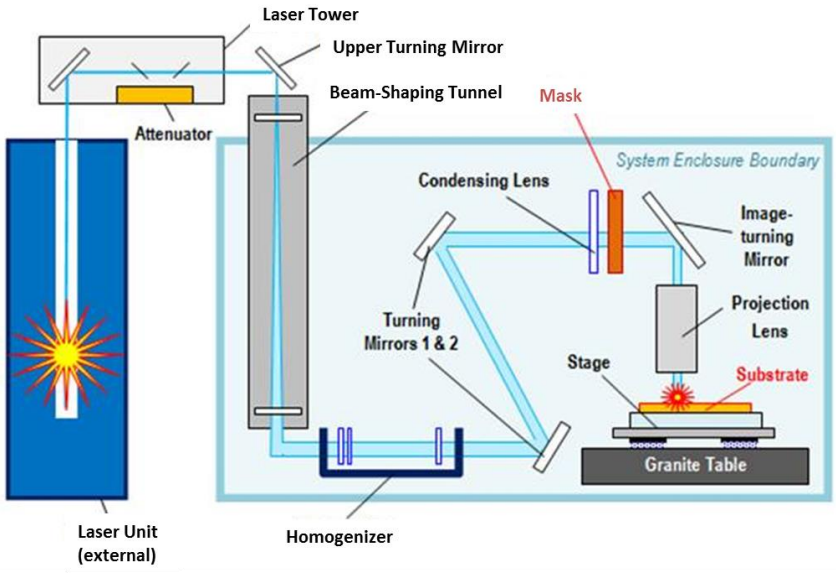

Figure 4.14 Example of beam delivery system schematic for an excimer laser ablation tool

4.1.2.2 Trench and Micro-via Formation by Excimer Laser Ablation

Trenches were formed in 15 µm thick GX92 films using the mask projection excimer laser process. The depth of the ablated trench can be controlled by changing the number of laser pulses. The trench depths for various laser pulses (5, 7, 8, 9 shots) at 800 mJ/cm^2 were measured and plotted in Figure 4.15. It was confirmed that the ablation depth and number of laser pulses had a linear relationship.

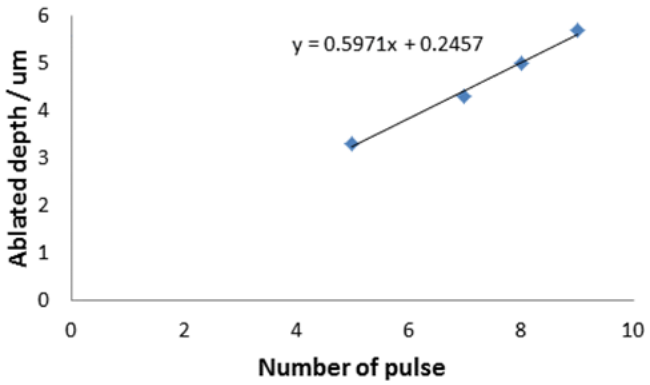

Figure 4.15 Ablated depth of trench with different number of laser pulses

After the formation of trenches, micro-vias were also drilled by excimer laser ablation. First, trenches with 10 µm width and 5 µm depth were created in 15 µm thick GX92 with nine pulses of mask projection excimer laser ablation. Thereafter, using a second mask, 10 µm deep micro-vias with 8 µm diameter were formed using twenty five pulses of laser ablation. The top view and profile of the structure are shown in Figure 4.16. No damage in the bottom copper pad was observed, and the micro-via side wall angle was measured to be 75°.

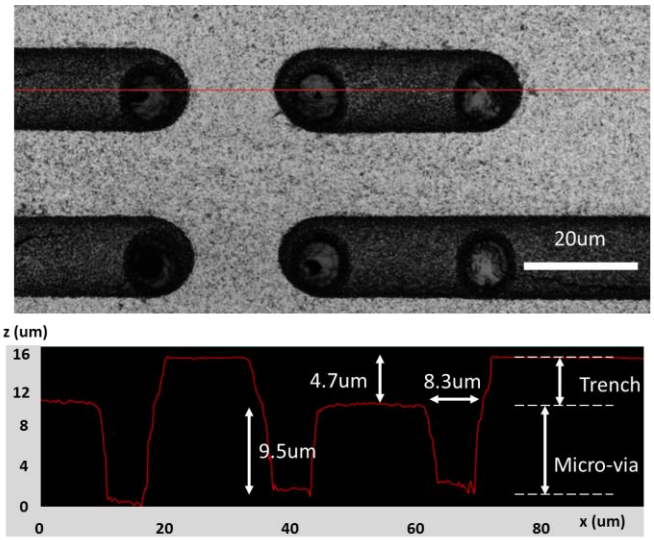

Figure 4.16 Top view and profile of the ablated trench and micro-via in GX92. The profile was measured at the red line in the top view

4.2 Metallization and Planarization of Trenches and Micro-vias

After the trench and micro-via formation, these structures were filled with copper by electrolytic plating processes. Finally, the excess amount of copper overburden was removed by surface planarization equipment by DISCO Japan, as an effective alternative to conventional CMP.

4.2.1 Effect of Plating Configuration on Metallization

Before the metallization step, cleaning processes were applied to the samples to remove residual debris sitting on the surface during the laser process. A chemical desmear process was used for the samples. Metallization of the trenches and vias were carried out with metal seed deposition by Eless Cu plating, followed by electrolytic plating. After the seed deposition processes, trenches and vias were filled with copper by

electrolytic plating. To achieve effective filling in the trenches and vias, right selection of plating chemistry and electrolyte flow is very critical, and two different configurations of plating processes were examined in this research. One configuration used Cupracid TP™ by Atotech, Germany and nozzles facing parallel to the samples (process tank A), while the other configuration used Inpro THF™ by Atotech and nozzles facing perpendicular to the samples (process tank B). Nozzles with parallel orientation create a laminar flow on the surface, whereas ones with perpendicular orientation create turbulence. The samples had trenches with 20 µm width, 60 µm length and 5 µm depth. After 40 minutes of electrolytic copper plating at 10 A, profiles of the plated trenches were observed with an optical profiler (Figure 4.17), and copper thickness on the sample surface was measured with an electrical thickness gauge. From tank A, plated copper thickness on the surface was 5 µm and the depth of the dimple was 3.2 µm. From tank B, copper thickness on the surface was 6 µm and the depth of the dimple was 0.2 µm. This result indicates the process with tank A was closer to conformal plating, whereas the process with tank B was more of a trench fill plating. Plating with tank B had an advantage in effective copper filling in trenches without depositing thick copper on top of the surface.

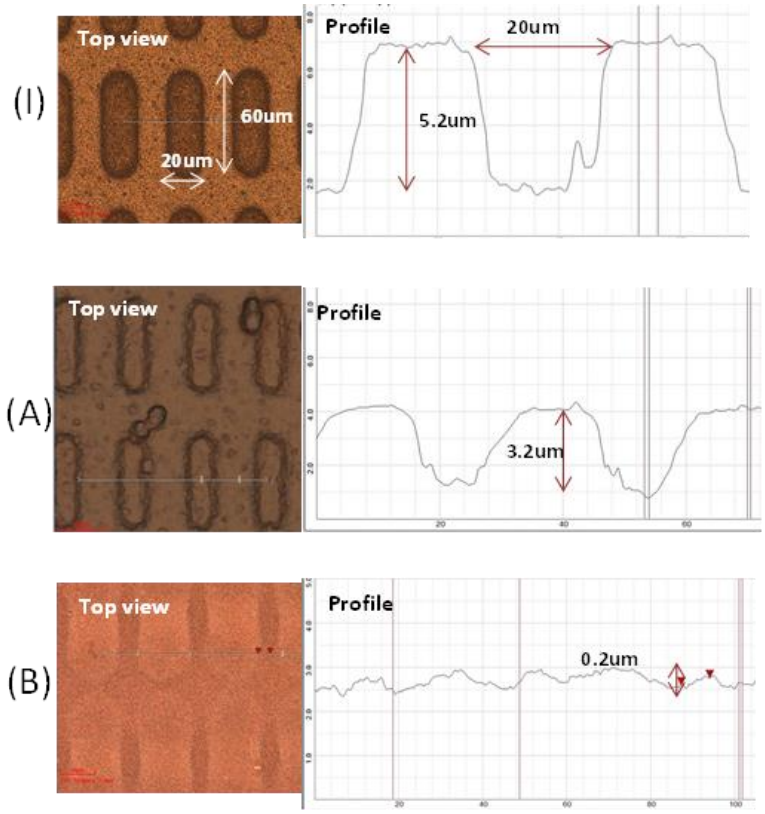

Figure 4.17 Trench filling by different electrolytic plating processes. (I): before plating, (A): after 40 min plating at 10 A with tank A, (B): after 40 min plating at 10 A with tank B

4.2.2 Copper Overburden Removal by Cutting Surface Planarization

After filling of the trenches and vias by plating processes, the copper overburden on the surface needs to be removed to form the final RDL structure. Copper wet etching is the simplest method, however, control of the etching thickness to micron and sub-micron uniformity across large panels is extremely challenging. Given the as-plated complex surface profiles, wet etching process poses a high risk of over-etching into the embedded copper trenches. Chemical Mechanical Polishing (CMP) is a well-established process to remove copper overburden from the surface on silicon wafers. However, as

mentioned earlier, the process cost of ownership (CoO) is high and scaling to large panel manufacturing is extremely challenging. In this research, a newly developed surface planer process tool from DISCO Japan was used for the planarization and removal of the overburden, because of lower CoO and scalability to panel-base manufacturing due to its simplicities in the equipment kinematics. The surface planer process can effectively remove ductile materials such as metals and/or polymers from the surfaces of substrates. The process point consists of a single bit made of diamond, which is mounted on a spindle rotating at high speed at a fixed height. The substrate is fixed on a flat chuck table that is creep-fed under the rotating bit that is barely contacting the surface (Figure 4.18). The surface of the chuck table is in precise parallelism with the plane defined by the rotation of the processing bit. As the tool shaves the substrate, the unevenness of the ductile material on the surface is carved off, leaving an extremely flat surface with excellent total thickness variation (TTV) control across the substrate. In case of this study, the copper overburden was removed in this fashion.

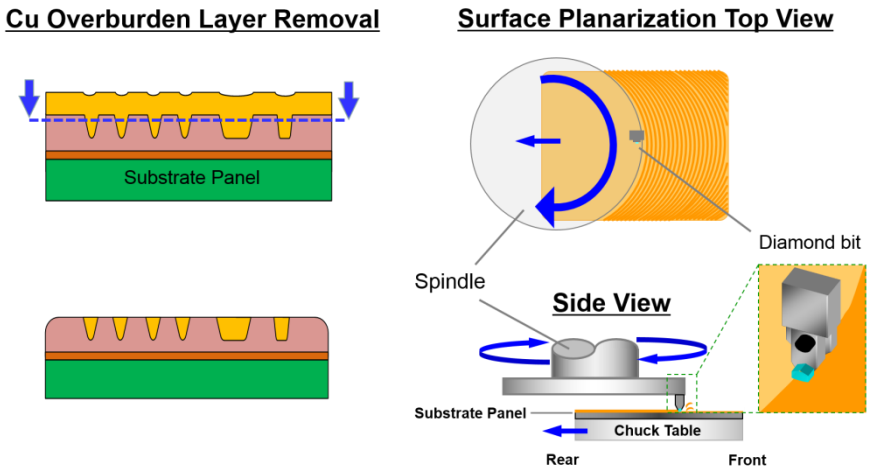

Figure 4.18 Illustration of Cu overburden removal by a surface planarization process

Thickness variations within a sample can affect the precise cutting of the plated surfaces. To illustrate the impact of total thickness variation (TTV) of core materials on planarization, two samples with different core substrates were prepared. First, 15 µm thick ABF GX92 films were laminated on both 6 inch × 6 inch square FR-4 (700 µm thick) and glass (500 µm thick) panels. The TTV of the FR-4 panel was 4 µm, while that of the glass panel was 1 µm. In the laminated ABF layers, trenches with 4 µm depth were formed by excimer laser ablation. Subsequently, trenches were filled with copper by electroless and electrolytic plating processes. The surface planer tool was used to remove copper overburden from the samples, and the inspection results are shown in Figure 4.19. In the sample with the FR-4 core, residual copper can still be observed in some devices in the center of the panel, while adjacent die areas were already showing signs of over-cutting. This is because of the unevenness of the FR-4 core. In contrast, more uniform cutting was observed in the sample with glass core, which has a much lower TTV. Some residual copper was seen at the edge of the glass sample, which was due to the edge setup in the plating process. These results indicate that a low TTV core, or co-planar base layer treatment, is critical for fine line RDL formation.

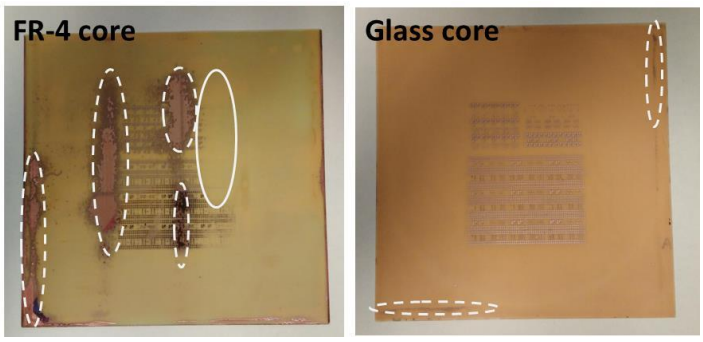

Figure 4.19 Top view of the 6 inch panels with FR-4 core (left), and glass core (right) after trench planarization. Circles with dashed line show residual copper and circles with solid line show overcut areas

Higher magnification images of the four corner coupons in the glass core sample are shown in Figure 4.20.

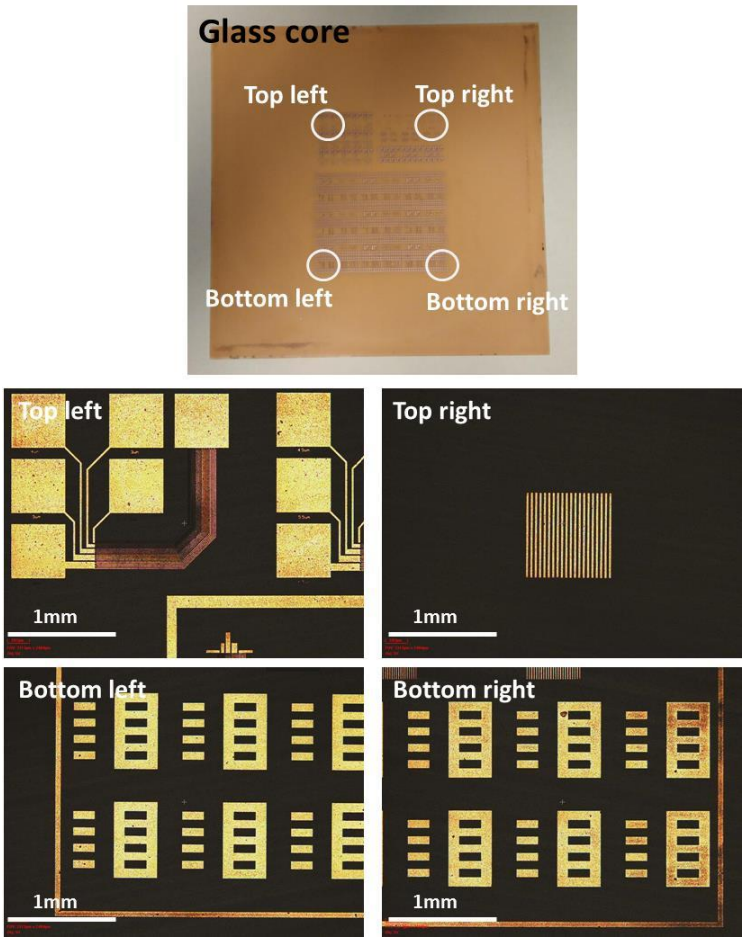

Figure 4.20 Magnified images of the four corner coupons in the glass core sample

The process research in this dissertation demonstrated a new embedded trench approach using excimer laser ablation, copper plating, and Disco's cutting surface planarization. The process flow is summarized in Figure 4.21.

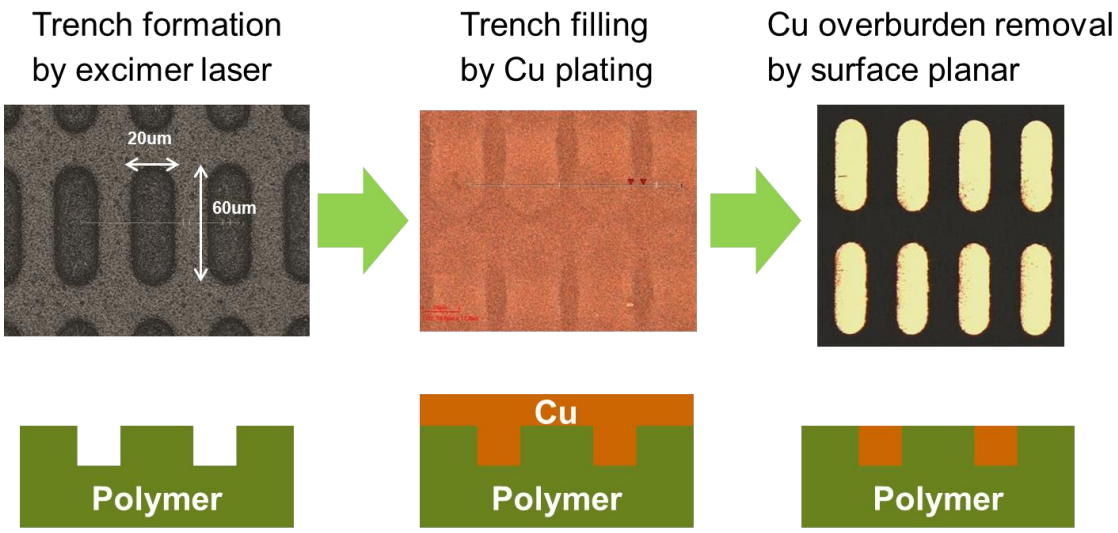

Figure 4.21 Developed embedded trench process scheme

4.3 Effect of Fillers in the Polymer Dielectric Material on Trench Profiles

Small trench formation is challenging in the traditional polymer dielectrics where large filler particles are included. However, no specific investigation has been previously conducted to understand the specific impact of the filler size. To investigate the effect of filler size in polymer dielectrics on trench size and profile, excimer laser ablation in different dielectric materials with varying filler sizes and a non-filled material was explored. Three different dry film materials, GX92, Material B, and pre-imidized polyimide were examined in this research. GX92 is a compound material of epoxy polymer matrixes and inorganic fillers, being widely used in the packaging industry [103]. Material B has the same polymer backbone as Material A, but with nano-scale silica filler (well below 1 µm size) particles. Table 4.1 shows the properties of Material B compared to Material A and the conventional epoxy polymer dielectric. Some of the

properties of Material B were different from Material A due to less filler content in Material B. High loading of smaller sized filler faced challenge in dry film fabrication due to larger surface area and increase in varnish viscosity. For higher filler loading, optimization of surface treatment of filler materials will be required. Although the properties of Material B were not measured experimentally, some of the properties were able to be estimated using equations provided in chapter 3. Rule of mixture was used for estimation of CTE, electrical constant and dielectric loss. Halpin-Tsai equation was used for estimating Young's modulus of the material B. Importantly, Material B is expected to have quite similar adhesion properties as Material A, since Material A and Material B have the same polymer architecture. For a non-filled dielectric, a pre-imidized polyimide material was selected in this research. Polyimide has been used for variety of packaging applications such as wafer level packaging and flexible substrates [104, 105]. Polyimide has strong absorption of UV light especially from 200 nm to 450 nm, which makes it superior in UV laser processing [106]. Polyimide is well known for its outstanding chemical, mechanical and thermomechanical properties because of the strong imide bonding and molecular packing. On the other hand, due to this strong molecular interaction, typical polyimide materials have very high melting point and are non-soluble in most of solvents, which makes it challenging to process the materials. Therefore, for the industrial use of polyimide materials, precursor polymers (polyamic acids) are molded or laminated first, then exposed to a thermal baking process to complete polyimide formation. For a dry film application, the thermal baking step has disadvantages such as requirement of high temperature (>300 °C) and large shrinkage during the baking. To address this issue, a new pre-imidized polyimide material by

Fujifilm was recently developed. This material can be manufactured as dry film type, processed by lamination step, and then cured at 200-250 °C [107].

Table 4.1 Properties of Material A and Material B (*: values were estimated from calculation)

Properties	Epoxy	Material A	Material B
Tg (°C)	153	162	161
CTE (ppm)	39	25	33*
Young's modulus (Gpa)	5.0	7.0	5.6*
Dk (at 1GHz)	3.2	3.0	2.7*
Df (at 1GHz)	0.018	0.006	0.009*
Water absorption with 100°C, 1h (%)	1.0	0.2	-

These polymer dielectric materials were studied to assess the impact of different filler sizes on small trench and micro-via formation. 15 µm thick GX92 and Material B were laminated with vacuum laminator at 100 °C on glass core materials, then oven cured at 180 °C. The polyimide film (8 µm thick) was laminated and cured with a hot press at 250 °C on glass core materials. These materials showed high material flow during the lamination process to achieve a flat surface over underlying copper circuitry. Figure 4.22 shows the surface topology of the three dielectric materials. In GX92, filler particles with diameter of around 1-2 µm were found, whereas filler size was 200-300 nm in Material B. Very smooth topology was observed on the polyimide surface due to the absence of filler particles.

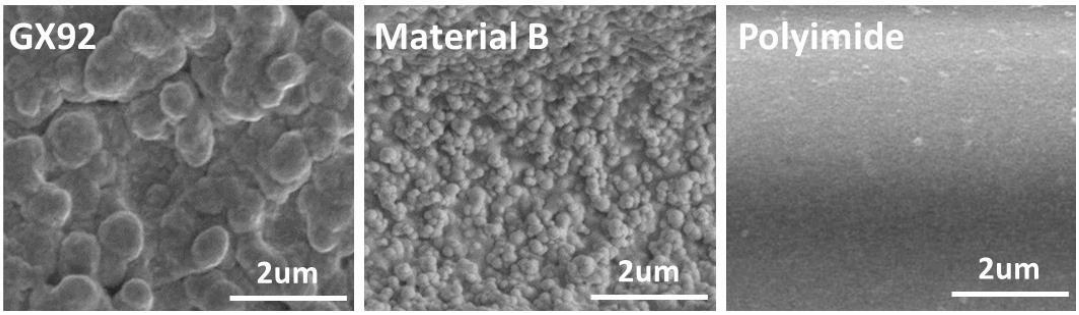

Figure 4.22 SEM images of the material surfaces

Trenches with 4 μm depth were formed in these dielectrics by excimer laser ablation under the same process conditions (nine pulses at 800 mJ/cm^2) using a mask with 2, 3, 4, and 5 μm line and space structures. Just after the excimer laser ablation, SEM micrographs (5000×) of the 4 μm width trenches in GX92 and Material B were prepared as shown in Figure 4.23. In spite of the difference in filler size, no huge difference in resolution was observed between these two materials. In all the cases, flat surfaces were observed at the top of the trench walls.

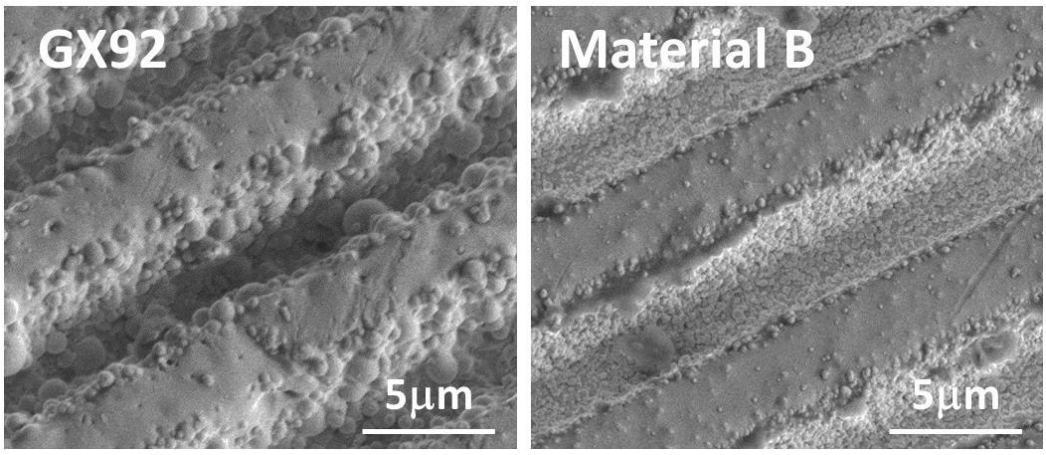

Figure 4.23 SEM images of 4 μm line and space trenches after excimer laser ablation in GX92 and Material B

After laser ablation, desmear cleaning processes need to be applied to remove polymer residues deposited on the surface. SEM micrographs of the same samples after desmear cleaning process were prepared and are shown in Figure 4.24. Plateaus on the trench walls observed in GX92 samples before desmear treatment have disappeared due to the severe side erosion and high roughness in trench side walls. Such high roughness in trenches can be explained on the basis of the ejection of large filler particles from the side walls during the desmear treatment, since the magnitude of the roughness in the trench side walls was approximately equal to the size of filler particles. The trench side wall roughness in Material B was significantly lower, due to the smaller size filler particles, and the side wall roughness was roughly equivalent to the filler particle size. As a result of reduced side erosion, flat surface on the trench walls in Material B was observed even after desmear treatment.

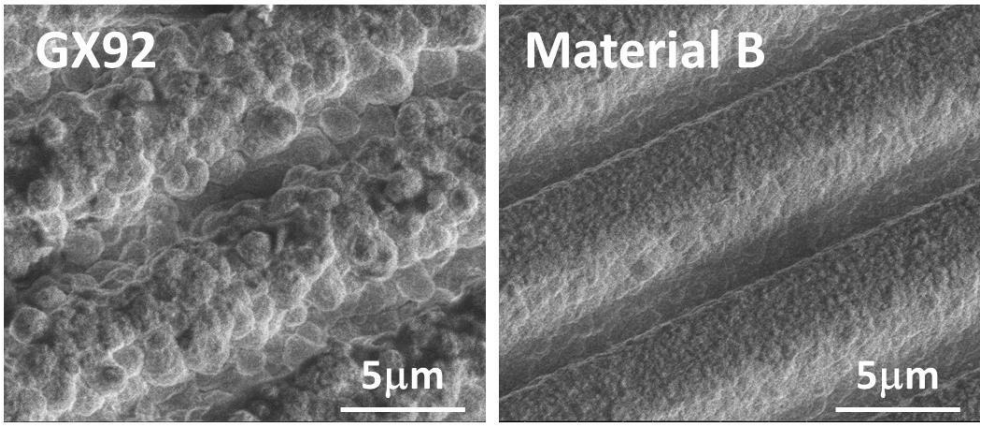

Figure 4.24 SEM images of 4 μm line and space trenches after desmear cleaning in GX92 and Material B

Figure 4.25 shows the SEM image of the 4 μm trenches in the pre-imidized polyimide material after acidic cleaning processes. The trench side walls in the polyimide material had the lowest surface roughness, which is consistent with the fact that the polyimide dielectric did not include any filler particles.

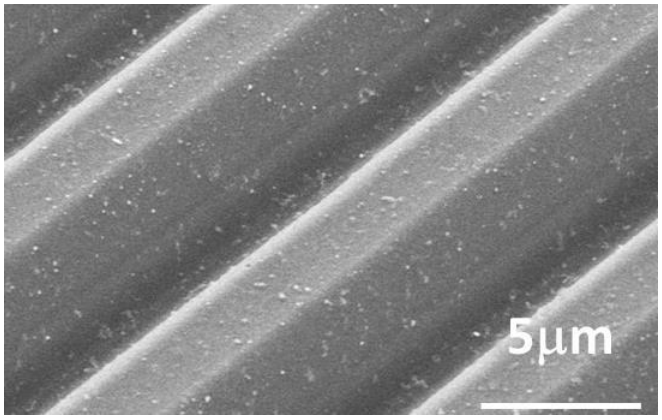

Figure 4.25 A SEM image of 4 μm line and space trenches after cleaning in pre-imidized polyimide

The profiles of the trenches in GX92, Material B, and pre-imidized polyimide after cleaning processes were measured with a laser confocal microscope. Profiles of the trenches are shown in Figure 4.26. Trench profile in GX92 was much rougher than that in Material B or polyimide. Additionally, trench walls in GX92 were collapsed due to the side erosion. Line and space trench structures down to 3 μm in Material B and down to 2 μm in polyimide were successfully formed.

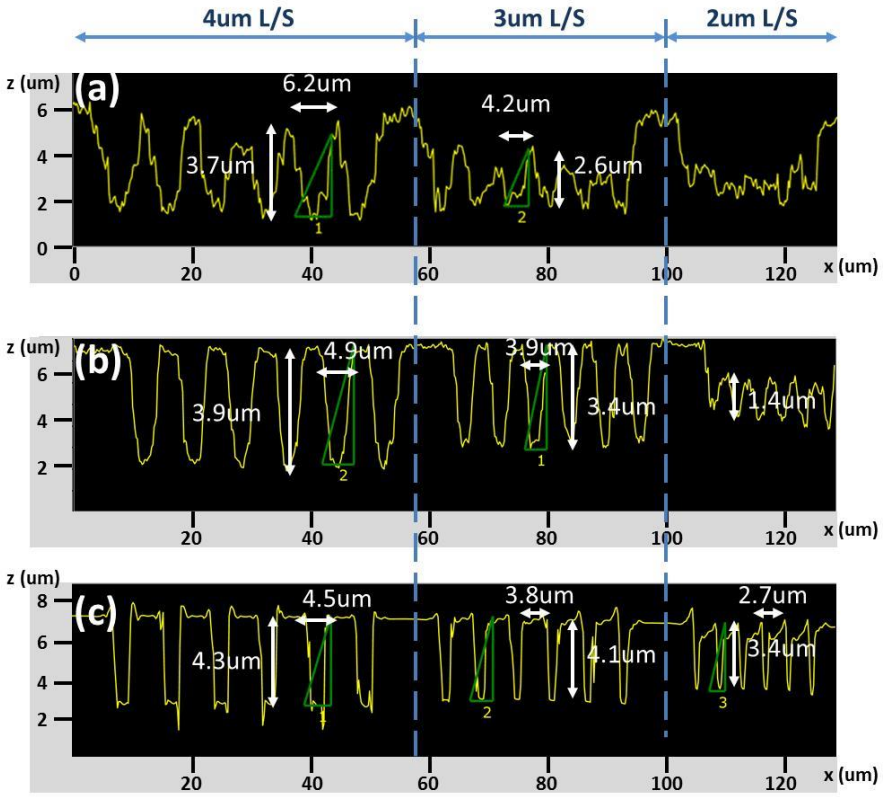

Figure 4.26 Line profile of 2, 3 and 4 µm line and space trenches in GX92 (a), Material B (b) and pre-imidized polyimide (c)

Due to large roughness and side erosion in GX92, trench width was extended by more than 2 µm on each side. As a result, trench structures below 5 µm line and space (10 µm pitch) could not be yielded in GX92. In contrast, side erosion of trenches in Material B was much smaller, below 0.5 µm on each side, which resulted in successful formation of trenches down to 2.5 µm line and space (5 µm pitch). In the case of polyimide, 2 µm line and space structures (4 µm pitch) were successfully demonstrated due to minimized side erosion. The SEM images of the smallest trench structures in each sample are shown in Figure 4.27.

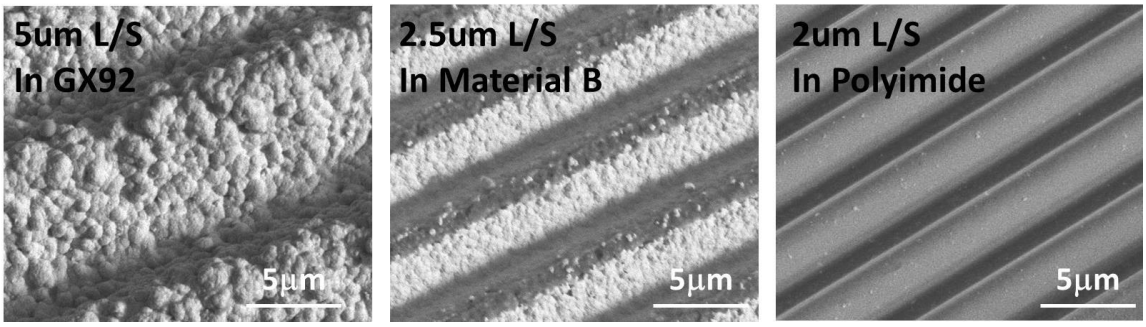

Figure 4.27 SEM images of the smallest trench structures resolved in different materials, 5 µm L/S in GX92 (left), 2.5 µm L/S in Material B (middle), and 2 µm L/S in polyimide

The relationship between the filler size and the smallest trench size achieved is plotted in Figure 4.28. A linear relationship was observed, which supports the fact that the amount of side erosion was of the same order as the filler particle size in the dielectric materials. The intercept value with y axis shows the minimum capability of the excimer laser resolution using the current system setup.

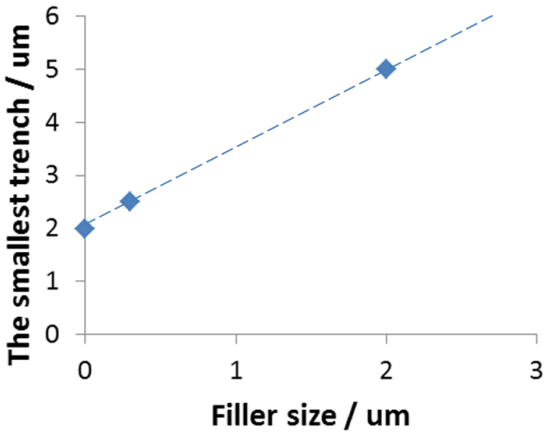

Figure 4.28 Filler size in the material vs. the smallest trench size resolved

Figure 4.29 shows the cross section view of the 2 µm line and space trench structure in pre-imidized polyimide, which has the highest aspect ratio of 1.4.

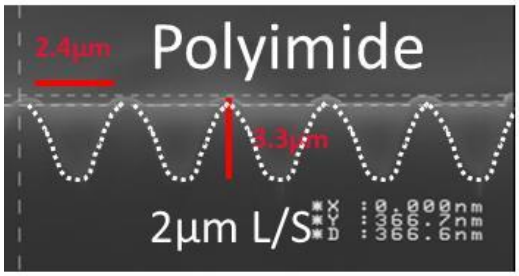

Figure 4.29 Cross sectional image 2 µm line and space trenches in pre-imidized polyimide

To form smaller and deeper trenches, side wall angles of the trenches should be increased, which can be achieved by laser ablation at higher fluence with modified optical set-up of the excimer laser system as previously reported (Figure 4.30). Due to the diffraction, laser beam becomes wider in size and weaker in power, as the beam goes deeper in materials and further from the focus point. Therefore, higher laser fluence can achieve more than threshold fluence for ablation at wider and deeper in the materials, leading to trench and micro-via formation with higher wall angles [108]. Equal to or more than 90° wall angle can be achieved in this fashion. Theoretical limit of the embedded trench approach can be calculated with Rayleigh's equation, defined as (resolution) = k × λ/NA, where k is the process factor, λ is the wavelength of the laser, and NA is the numerical aperture that represents the size of lends. In the current system, resolution was 2 µm using 308 nm wavelength laser with NA of 0.1 for optics. Therefore, k1 value can be calculated as 0.65 from the equation. Theoretically, NA (= n×sinθ, where n is the refractive index of air, θ is the incident angle) cannot be more than 1 in air.

Therefore, the theoretical limit of the resolution using the 308 nm excimer laser can be calculated as 200 nm. Reduction of trench size by the optimization of the optical set-up in excimer laser system can be achieved theoretically down to 200 nm, given the proper materials and processing.

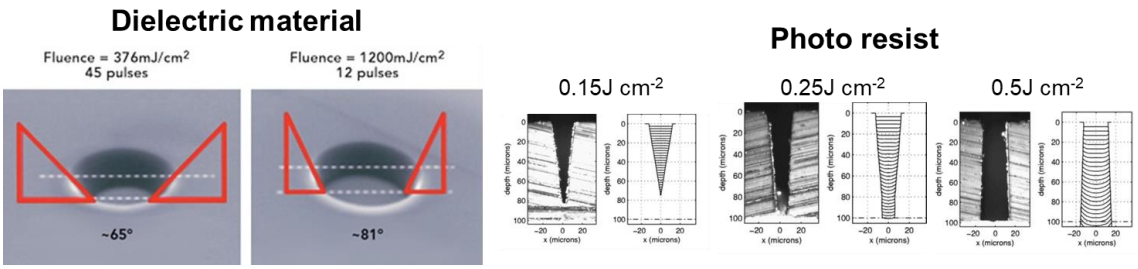

Figure 4.30 Increase in side wall angle with larger laser fluence (left: micro-vias in dielectric materials[109], right: trenches in photo resist materials[108])

To demonstrate metallized small trench structures, samples with polymer dielectrics on glass panels were prepared, and embedded trench processes, including excimer laser ablation, metallization, and planarization, were applied. Figure 4.31 shows the top view of the small trenches made by the processes. Trench structures with 5 μm width (10 μm pitch) on GX92, 2.5 μm width (5 μm pitch) on Material B, and 2 μm width (4 μm pitch) on polyimide materials were successfully achieved.

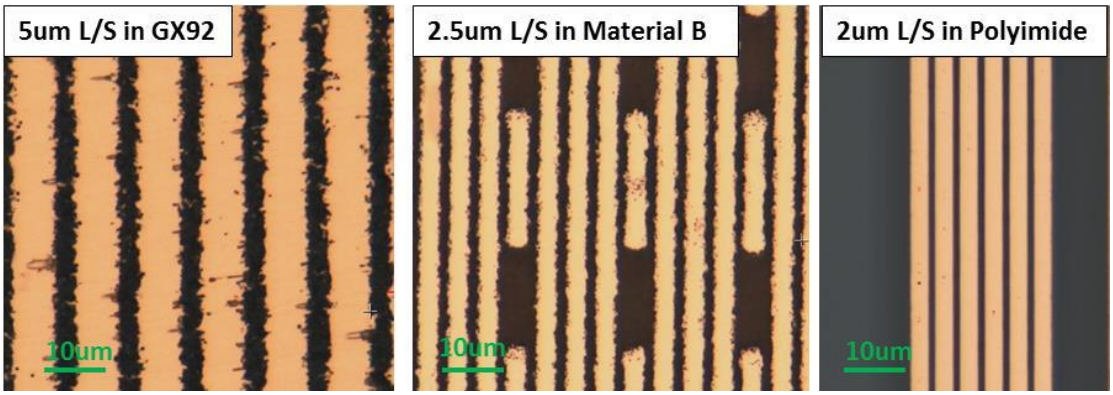

Figure 4.31 Fine pitch trenches formed in GX92 (left), Material B (middle), and polyimide (right)

4.4 Multi-layer RDL Demonstration and Reliability Testing

A sample with a multi-layer RDL structure was fabricated by repeating the process steps shown in Figure 4.1. An initial demonstration was conducted using GX92 polymer dielectric, excimer laser, and surface planarization processes. After the first embedded copper layer formation on GX92, a second metal layer was fabricated by lamination of a 15 µm thick GX92 film on top of the first copper layer. Thereafter, both trenches and vias were formed in the top dielectric layer by two steps of laser ablation. Then Eless copper plating and electrolytic copper plating were used for filling in the trenches and vias, followed by surface planarization to complete multi-layer fabrication. The top view and the cross section view of the fabricated daisy-chain structures with 20 µm pitch micro-vias is shown in Figure 4.32. Cross section pictures from different locations in a sample with lower magnification are shown in Figure 4.33. Highly planarized metal structures at large scale can be confirmed from the pictures, with via diameter of 8 µm and pad trench width of 15 µm.

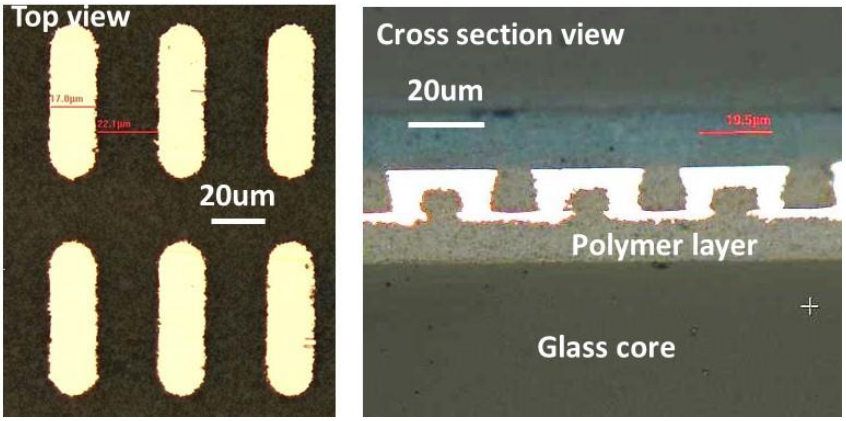

Figure 4.32 Top view (left) and cross section view (right) of the daisy-chain structure with 20 µm via pitch by embedded trace processes

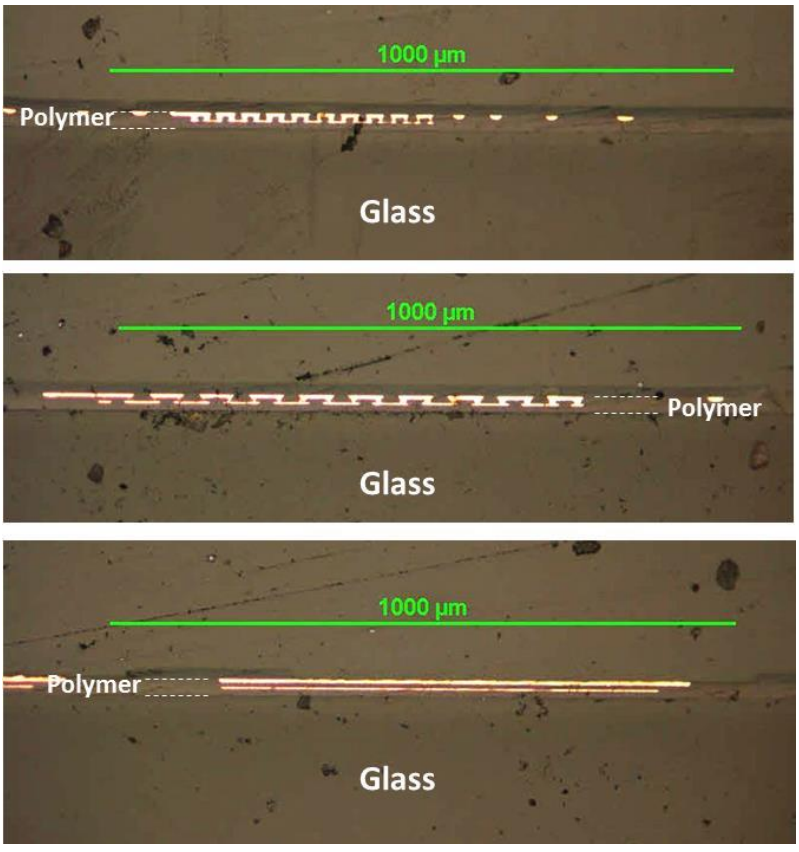

Figure 4.33 Cross section view of the multi-layer RDL of different locations in one sample

Daisy-chain coupons at three different via pitches (20, 30 and 40 µm) were fabricated and an initial reliability test was performed, according to a JEDEC standard, JESD22-A104D [41]. The electrical resistances of the daisy chain coupons with 100 micro-vias were measured before the test and after 100, 500, and 1000 cycles of liquid-to-liquid thermal shock test between -55 °C and 125 °C. The time zero resistance of the coupons with 20 µm via pitch was higher than those of 30 and 40 µm via pitches because the wiring widths in 20 µm pitch design were narrower; 15 µm wide for 20 µm pitch design and 20 µm wide for 30 and 40 µm pitch designs. No failure (failure criteria: 20% increase in resistance) was observed for all of the coupons up to 1000 cycles (Figure 4.34).

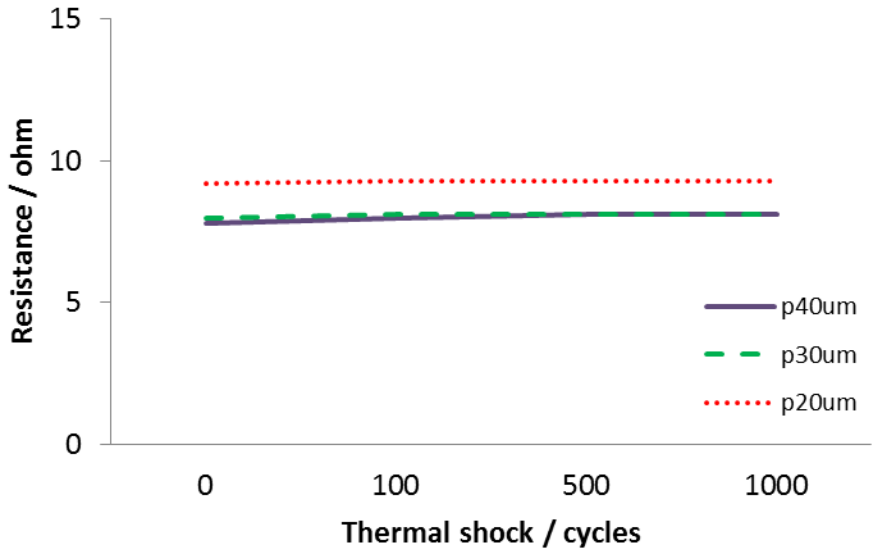

Figure 4.34 Daisy chain resistance (100 vias) of different via pitches under liquid-to-liquid thermal shock test (1 min at -55 °C, 1 min at 125 °C)

Multi-layer RDL daisy-chain test structures with smaller design rules were fabricated by the embedded conductor approach in Material B. Due to the small filler in the material, side erosion of the trenches and micro-vias were minimized to 1 µm, hence smaller pitch RDL structures were successfully demonstrated. Figure 4.35 shows the daisy-chain structure with 10 µm pitch embedded Cu wirings and micro-vias with 5 µm diameter and 5 µm depth. In this design, micro-via pitch was 20 µm, therefore, 5 µm width of dummy conductive lines were inserted in between the daisy-chain pads.

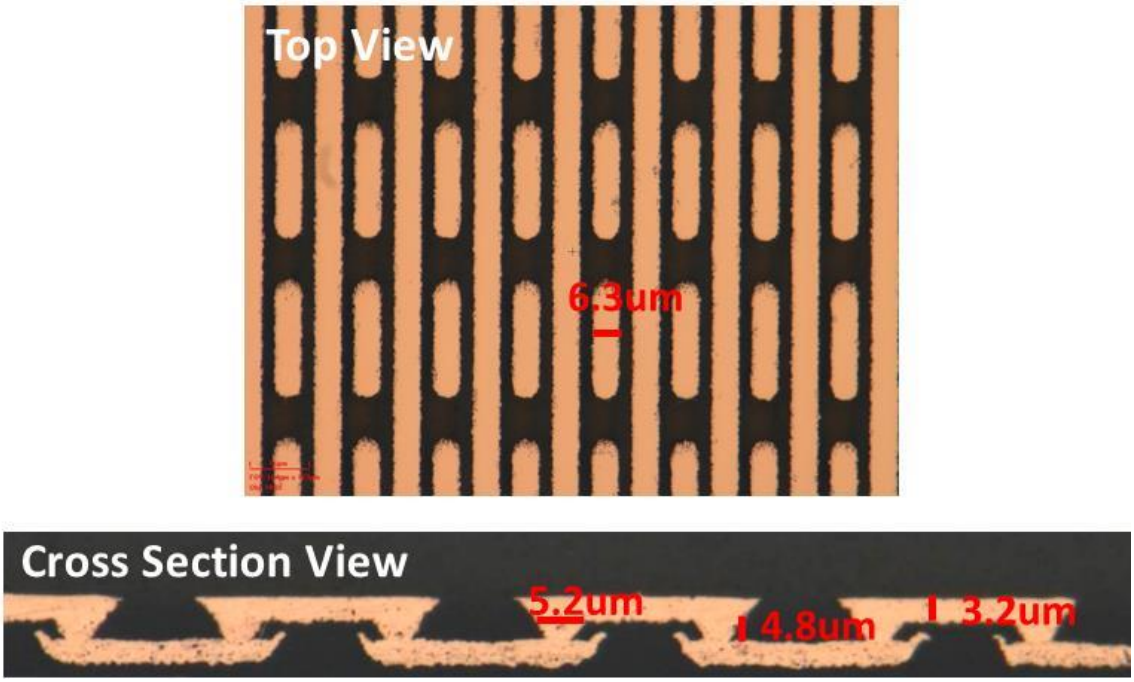

Figure 4.35 Top view (upper) and cross section view (lower) of the daisy-chain structure of the 5 µm line and space trenches and 5 µm diameter micro-vias

4.5 Chapter 4 Summary

This chapter described the research on exploration of new ultra-small micro-via and conductor wiring processes to form multilayer RDL structures at 20-40um pitch in ultra-thin dry film polymer dielectrics to address the scaling challenge of traditional SAP methods. Highly parallel mask projection processes with ozone etching and excimer laser ablation were investigated to form 2-5 μm wide trenches and 5-10 μm diameter micro-vias in 5-10 μm thin dry film polymer materials. Micro-via formation in thin polymer dielectrics by atmospheric ozone etching processes was successfully demonstrated first time in this research. However, micro-via diameter scaling below 10 μm and trench width scaling below 5 μm faced severe challenges due to the isotropic nature of the ozone etching process. In contrast, the efficient vertical ablation of polymer materials by an excimer laser enabled anisotropic etching of polymer layers and formation of small trenches and micro-vias. Detailed analysis of the effect of filler size on trench profile by excimer laser ablation revealed that the magnitude of the roughness in the trench side walls was created during the desmear treatment due to the ejection of filler particles. Hence, dielectric materials with smaller sized filler and non-filled dielectrics enabled small trench and micro-via structures due to minimized side wall erosion. As a result, trench structures with 2.5 μm line and space on Material B, and 2 μm line and space on polyimide materials were successfully achieved. Trench structures with highest aspect ratio of 1.4 were fabricated in pre-imidized polyimide. To form trenches with higher aspect ratio, laser ablation at higher fluence with modified optical set-up of the excimer laser system is required. After the trench and micro-via formation, these structures were filled with copper by electrolytic plating processes, followed by the

excess amount of copper overburden removal by surface fly cutting planarization process. Investigation of the impact of total thickness variation (TTV) on fly cut planarization revealed that a low TTV core with excellent co-planarity is critical for fine line RDL formation to achieve precise cutting of the plated surfaces. The process research in this dissertation demonstrated a new embedded trench approach using excimer laser ablation, copper plating, and Disco's cutting surface planarization.

CHAPTER 5. SUMMARY AND FUTURE WORK

This dissertation presented the first comprehensive research on ultra-thin dry film polymer dielectric materials and panel processes to form multilayer RDL structures at 20 μm I/O pitch on glass or other interposers. Although silicon interposers with back end of line (BEOL) RDL have been demonstrated with sub-micron lithography with 1-2 μm vias, they are limited by high electrical resistance due to thin SiO_2 dielectric and ultra-thin copper conductor traces, as well as high cost of each package from small 300mm wafers. Organic substrates on large panels using dry film polymer dielectrics are another approach being demonstrated, but their I/O pitch scaling has been limited by the thick dielectric layers and large vias, as well as large capture pads driven by poor dimensional stability of the organic cores. This research demonstrated a unique combination of ultra-thin polymer dielectric materials and processes for silicon BEOL like RDL dimensions, but scalable to large panels using dry film polymers and high aspect ratio processes for improved electrical performance, thus leading to both higher performance and lower cost than silicon interposers. The specific objective of this dissertation research was to explore 5 μm ultra-thin dry film polymer dielectric materials with the required properties, and processes to form 5 μm diameter micro-vias and 2 μm wiring lines with high positional accuracy of 1-2 μm to interconnect ICs at 20 μm bump pitch. Two major fundamental materials challenges were identified, (1) thin film polymer dielectric material with the required properties and (2) small micro-via and conductor wiring processes to form multilayer RDLs at 20 μm I/O pitch. The fundamental research focus was organized into two major tasks to address these challenges; (1) material design for electrical

performance and thermo-mechanical reliability, including strong adhesion, and (2) via and trench formation processes to achieve 20 μm I/O pitch multilayer RDL structures.

5.1 Research Summary

Task 1: Fundamental Material Design

To achieve the first target, the ideal dielectric material to form ultra-thin polymer layers was designed based on the analysis of required electrical, thermo-mechanical and adhesion properties. Fifty ohm impedance structures with 2 μm wiring traces were used to define the required dielectric thickness. Signal integrity assessment and finite element thermo-mechanical modeling (FEM) were conducted to address the required electrical, thermal and mechanical properties of the polymer dielectric materials. The material design led to new NP-epoxy copolymer dielectric material with the electrical and thermo-mechanical reliability performance. By incorporating the NP moiety into the epoxy unit, the insertion loss of the transmission signal was reduced in half of the traditional epoxy composite materials. Better CTE matching of the new material to copper and glass resulted in high thermo-mechanical reliability of the multi-layer RDL structures. Despite the inclusion of the less polar NP unit in the polymer backbone and the resulting smooth surface, the new material showed stable and high adhesion strength to electroless-plated copper seed layers. Detailed surface analysis of the material interface revealed that the strong adhesion with the smooth interface was attributed to the nanoscale roughness created at the interface. The topographic planarization capability of the 5 μm thin dry film material was evaluated, since the lithographic process to define small traces depends

highly on the degree of planarity (DoP) of the surface, and thinner dielectric layers pose additional challenges in achieving a planar surface over underlying copper traces. These investigations indicated the effectiveness of the dry film dielectric materials with NP-epoxy copolymer, however, there was a challenge in the line narrowing of fine pitch wirings by SAP process, which is critical for low line resistance.

Task 2: Ultra-Small Via and Trench Structure Formation Processes

To develop the RDL wiring process, a new embedded trench formation process was developed using parallel mask projection processes to address the challenges of RDL scaling by currently used semi-additive processes (SAP). In addition, an innovative planarization process was also demonstrated to alternate chemical-mechanical planarization (CMP). First, trench formation processes with atmospheric ozone etching and excimer laser ablation were investigated. While the formation of trench and micro-vias by ozone etching was isotropic, it was found that the trenches with high aspect ratio could be formed only by excimer laser ablation due to the anisotropic nature of laser ablation. The reduction of capture pad size was enabled by improving the positional accuracy of the micro-via formation processes with mask projection excimer laser ablation and by fabricating on dimensionally-stable glass core materials. In-depth analysis of the effect of filler size in the polymer dielectric on trench profiles, the impact of metallization processes and thickness variation of core materials were conducted to enable small trench formation below 5 μm with excimer laser and fly-cut planarization processes. The smallest trench width of 2 μm with an aspect ratio of 1.4 was achieved using the dielectric materials with nano-scale filler or non-filled materials. The smallest micro-vias with a diameter of 5 μm and depth of 5 μm were demonstrated by excimer

laser ablation as well. Further optimization of the laser system optics will be required to scale to structures below 2 μm width and with higher aspect ratios. Based on the material design and process research, multi-layer RDL structures were successfully fabricated and thermo-mechanical reliability of the stack-up was tested. The thesis research has successfully investigated a new class of dry film materials and scalable processes to meet the interconnection densities required for 2.5D interposers and packages. The research met the objective to explore 5 μm ultra-thin dry film polymer dielectric materials with desired properties, and processes to form 5 μm diameter micro-vias and 2 μm wiring with high positional accuracy of 1-2 μm.

5.2 Scientific and Technological Contributions

The following is a list of contributions of this dissertation.

- Provided a material design guideline for reliable RDL structures based on the thermo-mechanical analysis
- Evaluated the electrical and thermo-mechanical performance of NP-epoxy copolymer dielectric materials in package substrate application
- Analyzed the bonding mechanism of the Eless plated copper to NP-epoxy copolymer dielectric materials with low surface roughness
- Investigated small micro-via and trench formation processes with atmospheric ozone etching and excimer laser ablation to demonstrate small micro-via and trench less than 10 μm

- Analyzed the impact of filler size, metallization processes and core materials to enable small trench formation below 5 μm
- Demonstrated multi-layer RDL structures to test the initial reliability using newly designed materials and processes

5.3 Future Work

This dissertation left and raised many questions for further research. The first topic is an exploration of the performance and reliability of the multi-layer RDL structures with ultra-small structures. This dissertation has successfully provided the components for miniaturized RDL structures, such as 5 μm thin dry film polymer dielectric, 2 μm width wirings, and 5 μm diameter micro-vias. Electrical performance and reliability of the multi-layer RDL structure that comprises these small RDL structures are of great interest for 2.5D interposers and packages applications. The second topic is the further miniaturization of the embedded trench RDL structures below 2 μm by optimization of the excimer laser conditions such as laser power and optical setup. Many factors other than filler size may need to be considered for high resolution of the trench structures made by excimer laser ablation at smaller dimensions below 1 μm, such as laser absorption by polymer, plume effect and laser focus.

5.4 Publications

This section summarizes the list of published research work derived from this dissertation study.

Journal Papers

- Y. Suzuki, R. Furuya, V. Sundaram, R. R. Tummala, "Demonstration of 10 μm Micro-vias in Thin Dry Film Polymer Dielectrics for High Density Interposers," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 5, issue 2, pp. 194-200, 2015

- Y. Suzuki, H. Habib, F. Wei, V. Sundaram, R. R. Tummala, " Embedded Trench RDL at 2-5 μm Width and Space by Excimer Laser and Surface Planer for 20-40 μm Pitch Interposers," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 7, issue 6, pp. 838-845, 2017

- Y. Suzuki, E. Snyder, C. Ji, S. Walther, A. Gupta, C. Gottschalk, V. Sundaram, R. R. Tummala, " Micro-via Formation in 5 μm Thick Dry Film Dielectric by Ozone Etch Processes," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, accepted, August 2017

- Q. Chen, Y. Suzuki, G. Kumar, V. Sundaram, R. R. Tummala, "Modeling, Fabrication, and Characterization of Low-Cost and High-Performance Polycrystalline Panel-Based Silicon Interposer With Through Vias and

Redistribution Layers," *IEEE Transactions on Components, Packaging, and Manufacturing Technology,* vol. 4, pp. 2035-2041, 2014

- S. Sitaraman, Y. Suzuki, F. Liu, N. Kumbhat, S. J. Kim, V. Sundaram, R. R. Tummala, " Ultraminiaturized WLAN RF Receiver Module in Thin Organic Substrate," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 4, pp. 1276-1283, 2014

- B. Sawyer, Y. Suzuki, Z. Wu, H. Lu, V. Sundaram, K. Panayappan, R. Tummala, "Design and Demonstration of Fine-Pitch and High-Speed Redistribution Layers for Panel-Based Glass Interposers at 40-μm Bump Pitch," *Journal of Microelectronics and Electronic Packaging*, vol. 13, pp. 128-135, 2016

- B. Sawyer, Y. Suzuki, R. Furuya, N. Chandrasekharan, T.C. Huang, V. Smet, K. Panayappan, V. Sundaram, R.R. Tummala, "Design and demonstration of a 2.5D glass interposer BGA package for high bandwidth and low cost, high reliability, and direct attach to system PWB," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, accepted July 2016

- V. Sukumaran, G. Kumar, K. Ramachandran, Y. Suzuki, K. Demir, Y. Sato, T. Seki, V. Sundaram, R. R. Tummala, " Design, fabrication, and characterization of ultrathin 3-D glass interposers with through-package-vias at same pitch as TSVs in silicon," *IEEE Transactions on Components, Packaging, and Manufacturing Technology,* vol. 5, pp. 786-795, 2014

Conference papers

- Y. Suzuki, S. Sitaraman, A. Goyal, F. Liu, N. Kumbhat, M. Hashimoto, R. Mori, T. Jimbo, V. Sundaram, R. Tummala, "Low cost system-in-package module using next generation low loss organic material," *62th IEEE Electronic Components and Technology Conference, (ECTC)* 2012, San Diego, CA, United States, pp. 1412-1417, 2012
- Y. Suzuki, "Advanced materials for High-Speed Circuit and Radio Frequency (RF) module Applications," *63th IEEE Electronic Components and Technology Conference, (ECTC)* 2013, Las Vegas, NV, United States, CPMT session, 2013
- Y. Suzuki, Y. Takagi, V. Sundaram, R. Tummala, "Thin polymer dry-film dielectric material and a process for 10 um interlayer vias in high density organic and glass interposers," *64th IEEE Electronic Components and Technology Conference, (ECTC)* 2014, Orlando, FL, United States, pp. 1427-1432, 2014
- Y. Suzuki, J. Brune, R. Senczuk, R. Patzel, R. Furuya, F. Liu, V. Sundaram, R. Tummala, "Demonstration of 20μm pitch micro-vias by excimer laser ablation in ultra-thin dry-film polymer dielectrics for multi-layer RDL on glass interposers," *65th IEEE Electronic Components and Technology Conference, (ECTC)* 2015, San Diego, CA, United States, pp. 922-927, 2015
- Y. Suzuki, H. Hichri, L. Seongkuk, M. Arendt, Y. Chen, C. Lee, F. Wei, O. Dimov, D. Arora, S. Malik, V. Sundaram, R. Tummala, "Embedded Trace RDL at 2-5um Width and Space by Excimer Laser, Cu Filling and Surface

Planarization for 20-40um pitch Interposers," *67th IEEE Electronic Components and Technology Conference, (ECTC)* 2017, Orlando, FL, United States, May 30 - June 2, 2017

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